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<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,J45

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27 27	DDR3 Termination	10/31/2012 J15_MLB
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29 29	Thunderbolt Host (2 of 2)	01/14/2013 T29_RR
30 30	Thunderbolt Mobile Support	01/14/2013 T29_RR
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33 34	DDC Crossbar	11/16/2012 J15_REFERENCE
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47 56	Debug Sensors	12/21/2012 CHANG_J45
48 58	Thermal Sensors	11/26/2012 CHANG_J45
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59 73	CPU VR12.5 VCC Power Stage	10/31/2012 J15_MLB
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65 80	Power FETs	10/31/2012 J15_MLB
66 81	Power Control 1/ENABLE	03/15/2013 CHANG_J45
67 83	eDP Display Connector	10/31/2012 J15_MLB
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0456	1	SCHEM,MLB,J45	SCH	CRITICAL	
820-3662	1	PCBF,MLB,J45	PCB	CRITICAL	

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0067	COMMON PARTS,MLB,J45	J45_COMMON
985-0045	DEV BOM,MLB,J45	J45_DEVEL:ENG
639-4822	PCBA,MLB,BETTER,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600_S
639-4823	PCBA,MLB,BETTER,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600
639-4828	PCBA,MLB,BETTER,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600_S
639-4829	PCBA,MLB,BETTER,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600
639-4834	PCBA,MLB,BETTER,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600_S
639-4835	PCBA,MLB,BETTER,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600
639-4840	PCBA,MLB,BEST,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600_S
639-4841	PCBA,MLB,BEST,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600
639-4846	PCBA,MLB,BEST,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600_S
639-4847	PCBA,MLB,BEST,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600
639-4852	PCBA,MLB,BEST,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600_S
639-4853	PCBA,MLB,BEST,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600
639-4858	PCBA,MLB,CTO,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600_S
639-4859	PCBA,MLB,CTO,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600
639-4864	PCBA,MLB,CTO,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600_S
639-4865	PCBA,MLB,CTO,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600
639-4870	PCBA,MLB,CTO,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600_S
639-4871	PCBA,MLB,CTO,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600

J45 BOM Groups

BOM GROUP	BOM OPTIONS
J45_COMMON	ALTERNATE,COMMON,J45_COMMON1,J45_COMMON2,J45_PROGPARTS
J45_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X16,S2_PWR:S0
J45_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45_PVB	BKLT:PROD,SENSOR_NONPROD:N
J45_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:DVT,TBTROM:PROG,TPAD_PSOC:PROG
J45_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,CAM_XTAL:YES
J45_DEVEL:FSB	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,SENSOR_NONPROD_R
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	CRW,SR18J,,PRQ,C0,2.0,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	CRW,SR18H,PRQ,C0,2.3,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	CRW,SR1BS,PRQ,C0,2.6,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QEWV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600_S	HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600_S	SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600_S	ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600_S	MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600	SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600	ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0067	1	J45 MLB BASE BOM	BASE	CRITICAL	BASE_BOM
985-0045	1	J45 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC_MASTER=J15_MLB SYNC_DATE=10/25/2012

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Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S3919	1	IC,EPROM,Falcon RIDGE(V13.9)J44/45	U2890	CRITICAL	TBTROM:PROG
337S4587	1	IC,TP PSOC, QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK
341S3856	1	IC,TRKPD/KYBD,PSOC(V225)	U4801	CRITICAL	TPAD_PSOC:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3902	1	IC,SMC-B1,EXT,V2.12A54,EVT,J45	U5000	CRITICAL	SMC_PROG:EVT
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK:MACRONIX
335S0812	1	IC,SPI SRL 50MHZ,FLASH,64MBIT,SOIC8	U6100	CRITICAL	BOOTROM_BLANK:NUMONYX
341S3763	1	IC,EFI ROM(VXXXX)PROTO 0,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3780	1	IC,EFI ROM(V0035)PRE-PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PRE-PROTO1
341S3793	1	IC,EFI ROM(V0041)PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3811	1	IC,EFI ROM(V00xx)PROTO 2,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3890	1	IC,EFI ROM(V0100)PROTO3-J45 &EVT-J45	U6100	CRITICAL	BOOTROM_PROG:EVT
341S3929	1	IC,EFI ROM(Vxxxx)DVT-J45	U6100	CRITICAL	BOOTROM_PROG:DVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7845	1	MBP BARCODE LABEL	LABEL	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0241		ALL	Cyntec alt to TFT
376S1032	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Elpida F die alt
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba (U2030, U7001)

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PAGE TITLE: BOM Configuration

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REVISION: <E4LABEL>

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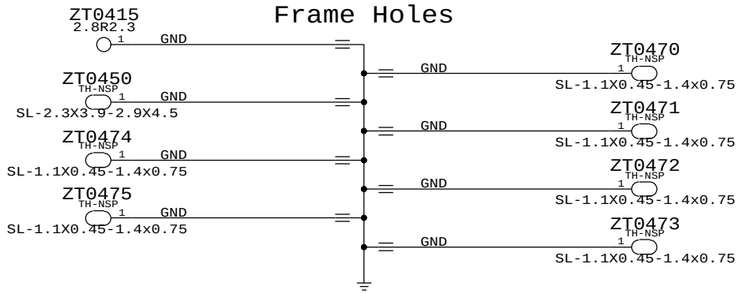
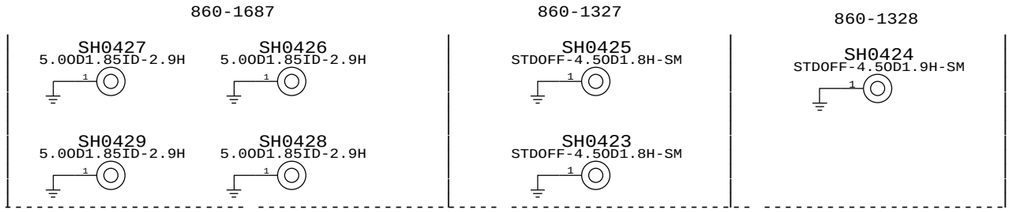
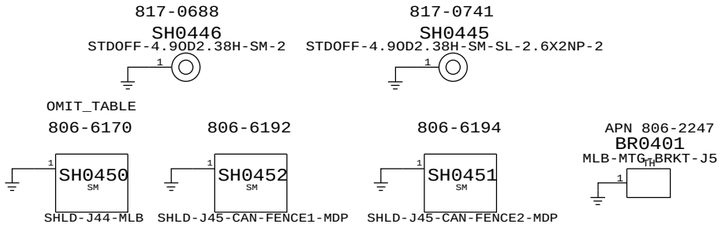
Frame Holes



J45 THERMAL MODULE STANDOFF





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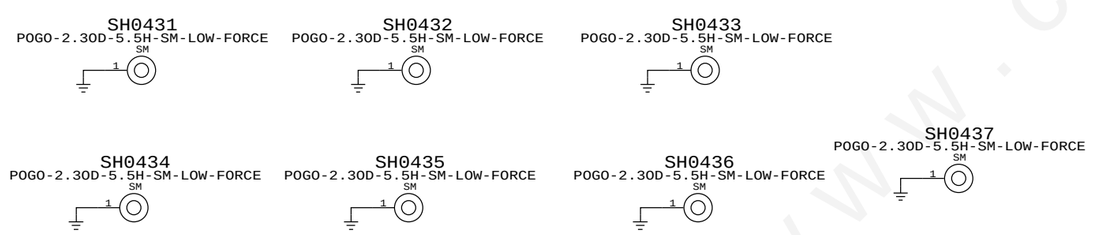

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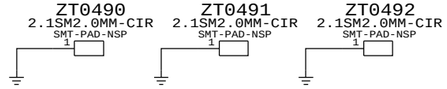
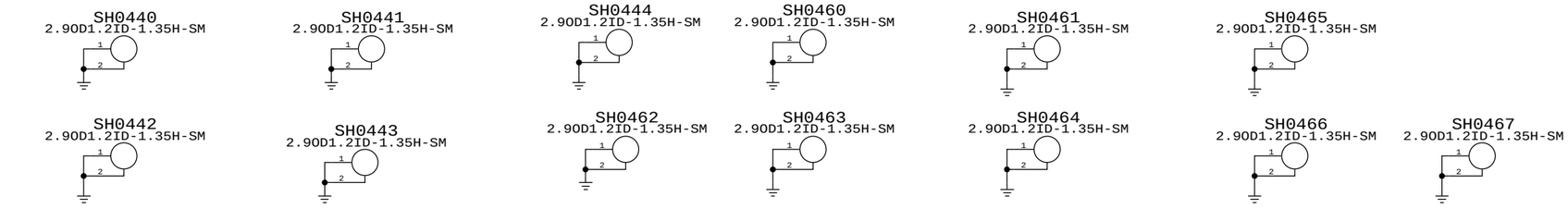


J45 StAND OFF

860-1448



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
725-1807	1	INSULATOR,REAR,MLB,J45	REAR_INSULATOR	CRITICAL	
725-1877	1	INSULATOR,CPU,J45	CPU_INSULATOR	CRITICAL	
725-1787	1	INSULATOR,PCH,J15	PCH_INSULATOR	CRITICAL	
806-6193	2	CAN COVER,mDP	CAN_COVER1, CAN_COVER2	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
806-9391	1	SHIELD CAN, USB,J45	SH0450	CRITICAL	

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PAGE TITLE: PD Parts

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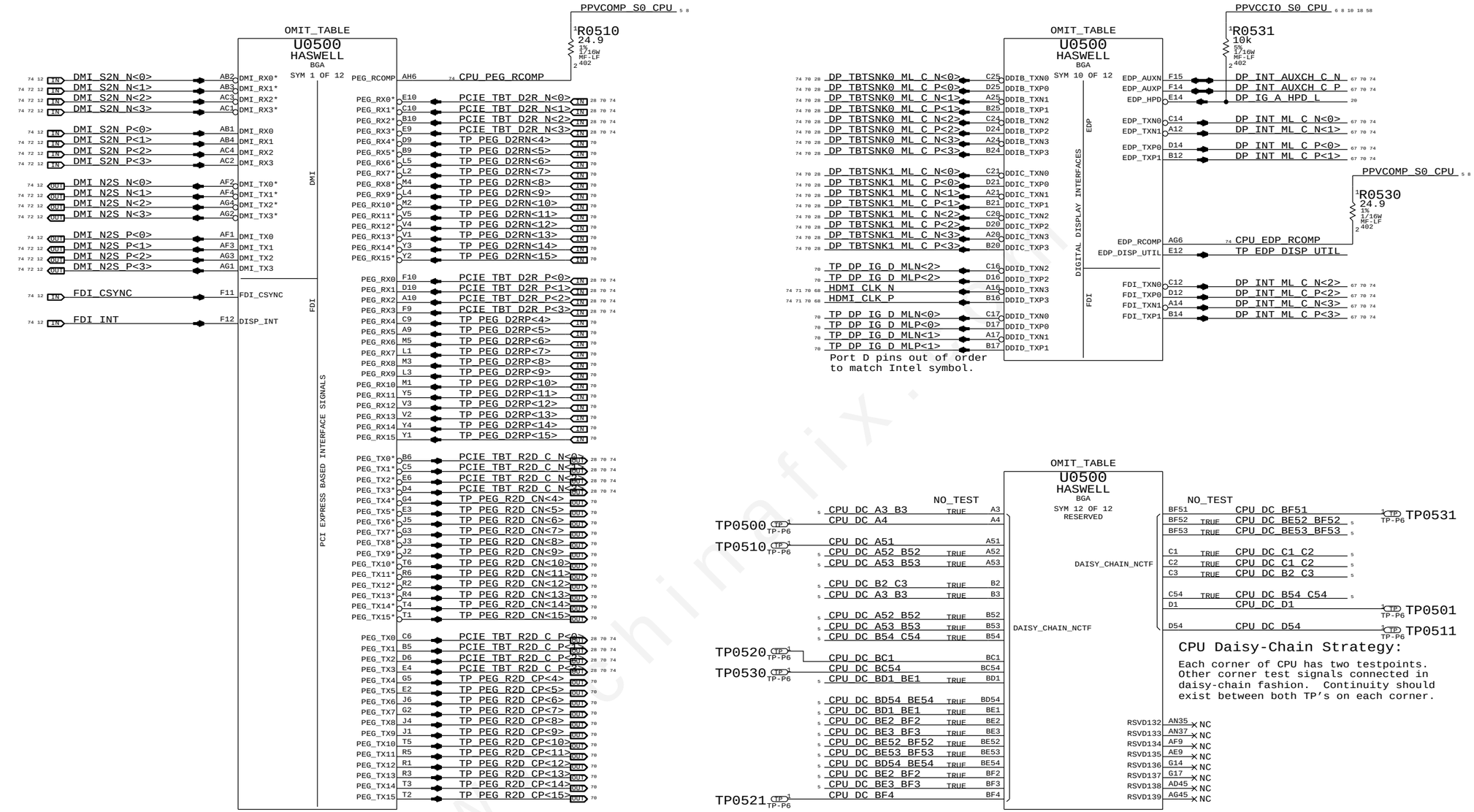

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PAGE TITLE

CPU DMI/PEG/FDI/RSVD

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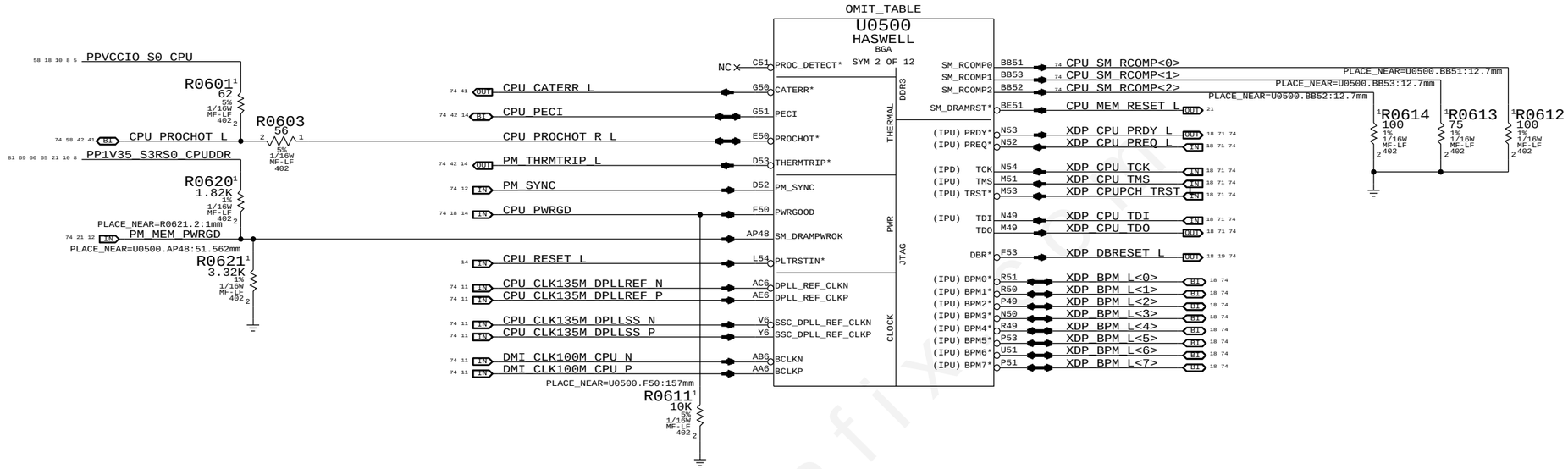
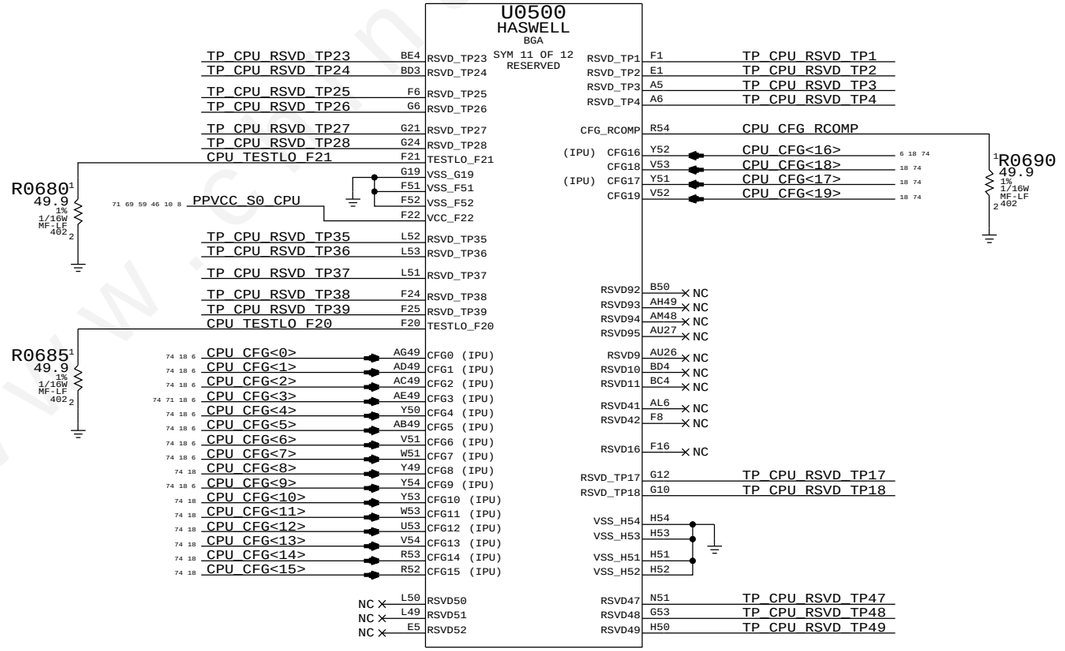
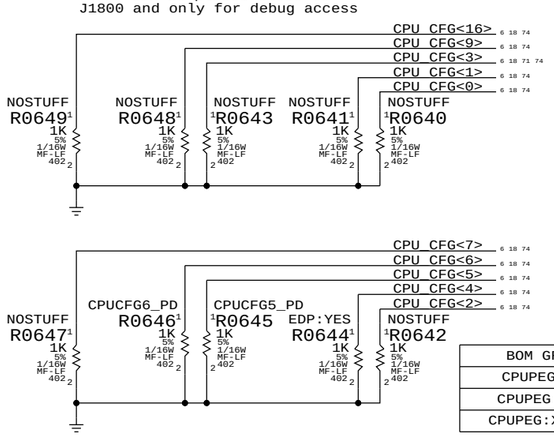




CFG [7] :PEG DEFER TRAINING — 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION — 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE — 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU Clock/Misc/JTAG/CFG

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OMIT_TABLE

U0500
HASWELL
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MEMORY CHANNEL A

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RSVD170	AU39	NC	

OMIT_TABLE

U0500
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SB_CKP3	AY27	NC	
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SB_DQS3	BE43	MEM_B_DQS_P<3>	
SB_DQS4	AW15	MEM_B_DQS_P<4>	
SB_DQS5	AW12	MEM_B_DQS_P<5>	
SB_DQS6	AW6	MEM_B_DQS_P<6>	
SB_DQS7	AL3	MEM_B_DQS_P<7>	
RSVD173	BD38	NC	
RSVD174	BF39	NC	
RSVD175	BE39	NC	
RSVD176	BF37	NC	
RSVD177	BE37	NC	
RSVD178	BD39	NC	
RSVD179	BC39	NC	
RSVD180	BC37	NC	
RSVD181	BD37	NC	

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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CPU DDR3 Interfaces

Apple Inc.

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NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

PPVCCIO_S0_CPU
Max load: 300mA MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

R0800 75 1% 1/10W MF-LF 402
R0802 110 1% 1/16W MF-LF 402
R0810 43 5% 1/16W MF-LF 402
R0811 0 5% 1/16W MF-LF 402
R0812 0 5% 1/16W MF-LF 402

CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT

R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

PPVCC_S0_CPU
R0860 100 1% 1/10W MF-LF 402
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM
CPU_VCCSENSE_P

PPVCOMP_S0_CPU
Max load: 300mA MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

PP1V35_S3RS0_CPUDDR

U0500
HASWELL
BGA
SYM 5 OF 12
OMIT_TABLE

NC	J17	RSVD64
NC	J21	RSVD65
NC	J26	RSVD66
NC	J31	RSVD67
	AR29	
	AR31	
	AR33	
	AT13	
	AT19	
	AT23	
	AT27	
	AT32	
	AT36	
	AV37	
	AW22	
	AW25	
	AW29	
	AW33	
	AY18	
	BB21	
	BB22	VDDQ
	BB26	
	BB27	
	BB30	
	BB31	
	BB34	
	BB36	
	BD22	
	BD26	
	BD30	
	BD33	
	BE18	
	BE22	
	BE26	
	BE30	
	BE33	
NC	AN31	RSVD68
	L6	VCC_L6
	M6	VCC_M6
NC	AN22	RSVD69
NC	AN18	RSVD70
	C50	VCC_SENSE
NC	AH9	RSVD71
	D51	VCCIO_OUT
NC	F17	FC_F17
	AK6	VCOMP_OUT
NC	AN33	RSVD72
NC	W9	RSVD73
NC	J12	RSVD79(VSS)
NC	AR49	RSVD74
	J53	VIDALERT*
	J52	VIDSCLK
	J50	VIDSOUT
	B51	VSS_B51
	F19	PWR_DEBUG
	E52	VSS_E52
	V49	RSVD75
	U49	RSVD76
	AM49	IVR_ERROR
	W49	RSVD78
	V50	VSS_V50(RSVD)
	AN49	VSS_AN49(RSVD)
	AJ49	VSS_AJ49(RSVD)
	AG50	VSS_AG50(RSVD)
	AK49	VSS_AK49(RSVD)
	AJ50	VSS_AJ50(RSVD)
	AP49	VSS_AP49(RSVD)
	AB50	VSS_AB50(RSVD)
	AP50	VSS_AP50(RSVD)
	AD50	VSS_AD50(RSVD)
	AM50	VSS_AM50(RSVD)
	A36	
	A38	
	A39	
	A42	
	A43	
	A45	
	A46	VCC
	A48	
	AA46	
	AA47	
	AA8	
	AA9	

CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_PWR_DEBUG
TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
TP_CPU_IVR_ERROR
TP_CPU_RSVD_TP78

PPVCC_S0_CPU

	B43	
	B45	
	B46	
	B48	
	C27	
	C28	
	C31	
	C32	
	C34	
	C36	
	C38	
	C39	
	C42	
	C43	
	C45	
	C46	
	C48	
	D27	
	D28	
	D31	
	D32	
	D34	
	D36	
	D38	
	D39	
	D42	
	D43	
	D45	
	D46	
	D48	
	E27	
	E28	
	E31	
	E32	
	E34	
	E36	
	E38	
	E39	
	E42	
	E43	
	E45	
	E46	
	E48	VCC
	F27	
	F28	
	F31	
	F32	
	F34	
	F36	
	F38	
	F39	
	F42	
	F43	
	F45	
	F46	
	F48	
	G27	
	G29	
	G31	
	G32	
	G34	
	G36	
	G38	
	G39	
	G42	
	G43	
	G45	
	G46	
	G48	
	H11	
	H12	
	H13	
	H14	
	H16	
	H17	
	H18	
	H19	
	H20	
	H21	
	H23	
	H24	
	H25	
	H26	
	H27	
	H29	

Connections would be required
for 2014 CPU support.

FC_D5	D5	TP_CPU_FC_VCCST
FC_D3	D3	TP_CPU_FC_VCCST_PWRGD

OMIT_TABLE
U0500
HASWELL
BGA
SYM 6 OF 12
POWER

| | | |

OMIT_TABLE

U0500
HASWELL
BGA
SYM 7 OF 12
GROUND

A11	VSS	AJ48
A15		AJ51
A19		AJ54
A22		AK48
A26		AK5
A30		AK50
A33		AK7
A37		AK9
A40		AL1
A44		AL4
AA1		AL48
AA2		AL5
AA3		AL7
AA4		AM5
AA48		AM51
AA5		AM52
AA7		AM53
AB5		AM54
AB51		AM7
AB52		AN1
AB53		AN2
AB54		AN3
AB7		AN4
AB9		AN48
AC48		AN5
AC5		AN50
AC50		AN7
AC7		AP51
AD48		AP54
AD51		AP7
AD54		AR12
AD7		AR14
AD9		AR16
AE1		AR18
AE2		AR20
AE3		AR24
AE4		AR26
AE48		AR48
AE5		AR5
AE50		AR50
AE7		AR7
AF5		AR8
AF6		AR9
AF7		AT1
AG48		AT10
AG5		AT12
AG51		AT15
AG52		AT16
AG53		AT18
AG54		AT20
AG7		AT22
AG9		AT25
AH1		AT26
AH2		AT29
AH3		AT33
AH4		AT35
AH48		AT37
AH5		AT39
AH50		AT4
AH7		

OMIT_TABLE

U0500
HASWELL
BGA
SYM 8 OF 12
GROUND

AT40	VSS	AY50
AT42		AY9
AT43		B11
AT45		B15
AT46		B19
AT47		B22
AT49		B26
AT5		B30
AT50		B33
AT51		B37
AT52		B40
AT53		B44
AT54		B49
AT6		B8
AT8		BA13
AT9		BA18
AU13		BA22
AU18		BA25
AU22		BA29
AU25		BA33
AU29		BA37
AU33		BA4
AU37		BA42
AU42		BA5
AU5		BA50
AU9		BA51
AV1		BA52
AV13		BA53
AV18		BA9
AV2		BB10
AV22		BB11
AV25		BB12
AV29		BB14
AV3		BB15
AV33		BB16
AV4		BB17
AV42		BB18
AV5		BB20
AV50		BB23
AV9		BB25
AW13		BB28
AW18		BB32
AW37		BB33
AW42		BB37
AW43		BB38
AW45		BB39
AW46		BB41
AW47		BB42
AW49		BB43
AW5		BB44
AW50		BB46
AW51		BB47
AW54		BB48
AW9		BB49
AY13		BB5
AY22		BB6
AY25		BB7
AY29		BB9
AY33		
AY37		
AY42		

OMIT_TABLE

U0500
HASWELL
BGA
SYM 9 OF 12

G20	VSS	AR22	VSS_AR22(RSVD)	A49	VSS_NCTF	D50	VSS_SENSE
G23		AB48	VSS_AB48(RSVD)	A50			
G25		P9	VSS_P9(RSVD)	A8			
G26		G18	VSS_G18(RSVD)	B4			
G30				BA1			
G33				BA54			
G37				BB1			
G40				BB54			
G44				BD2			
G49				BD53			
G52				BF49			
G54				BF5			
G7				BF50			
G8				BF6			
G9				C53			
H44				D2			
H49				E54			
H7				F54			
J44				G1			
J49							
J51							
J54							
J7							
K1							
K2							
K3							
K4							
K5							
K6							
K7							
L48							
L7							
L9							
M48							
M50							
M52							
M54							
M7							
N48							
N7							
P1							
P2							
P3							
P4							
P48							
P5							
P50							
P52							
P54							
P6							
P7							
R48							
R7							
T48							
U1							
U2							
U3							
U4							
U48							
U5							
U50							
U52							
U54							
U6							
U7							
V48							
V7							
V9							
W48							
W50							
W52							
W54							
W7							
Y48							
Y7							
Y9							

BC10	VSS	F11
BC12		F15
BC15		F16
BC18		F17
BC22		F19
BC26		F20
BC3		F21
BC30		F22
BC33		F24
BC36		F25
BC38		F26
BC41		F29
BC43		F33
BC46		F37
BC48		F4
BC5		F40
BC50		F44
BC52		F49
BC7		F5
BD10		G11
BD15		G13
BD18		G16
BD36		
BD41		
BD46		
BD5		
BD51		
BE10		
BE15		
BE36		
BE41		
BE46		
BF10		
BF12		
BF15		
BF18		
BF22		
BF26		
BF30		
BF33		
BF36		
BF38		
BF41		
BF43		
BF46		
BF48		
BF7		
C11		
C15		
C19		
C22		
C26		
C30		
C33		
C37		
C4		
C40		
C44		
C49		
C52		
C8		
D11		
D15		
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D22		
D26		
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D40		
D44		
D49		
D8		
E11		
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E44		
E49		
E51		
E53		
E8		
F2		
F26		
F3		
F30		
F33		
F37		
F4		
F40		
F44		
F49		
F5		
G11		
G13		
G16		

CPU_VCCSENSE_N
OUT 58 74

R0960
100
5%
1/16W
MF-LF
402
PLACE_NEAR=U0500.D50:50.8mm
PLACE_SIDE=BOTTOM

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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CPU Ground

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 8x 210uF(2x nostuff) 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1001 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1002 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1020-C1023):
CAPs for Acoustic control (C109A-C102D)
Place near U0500 on bottom side

C1020 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1021 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1022 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1023 20UF 20% 4V X5R-CERM 0402-2
C109A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

CRITICAL C1024 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1025 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1026 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1027 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1028 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1029 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1030 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1031 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1032 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1033 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1034 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1035 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1036 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1037 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1038 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1039 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1040 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1041 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1042 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1043 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1044 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1045 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

CRITICAL C1046 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1047 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1048 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1049 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1050 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1051 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1052 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1053 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1054 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1055 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1056 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1057 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1058 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1059 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1060 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1061 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1062 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1063 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1064 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1065 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1066 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1067 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1068-C1076:
CAPs for Acoustic control (C102E-C103F)

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1069 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1070 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1071 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1072 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1073 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1074 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1075 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1076 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1077 210UF 20% 2.5V POLY-TANT CASE-B2S

C102E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

PLACEMENT_NOTE (C1080-C1089):

PP1V35_S3RS0_CPUDDR

Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603
C1091 10UF 20% 4V X6S-CERM 0603
C1092 10UF 20% 4V X6S-CERM 0603
C1093 10UF 20% 4V X6S-CERM 0603
C1094 10UF 20% 4V X6S-CERM 0603
C1095 10UF 20% 4V X6S-CERM 0603
C1096 10UF 20% 4V X6S-CERM 0603
C1097 10UF 20% 4V X6S-CERM 0603

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 2.5V POLY-TANT D1ST-ECGLT-COMBO
CRITICAL C1099 330UF-6MOHM 20% 2.5V POLY-TANT D1ST-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

PPVCCIO_S0_CPU

C1079 0.01UF 10% 10V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 10 OF 118
SHEET: 10 OF 81

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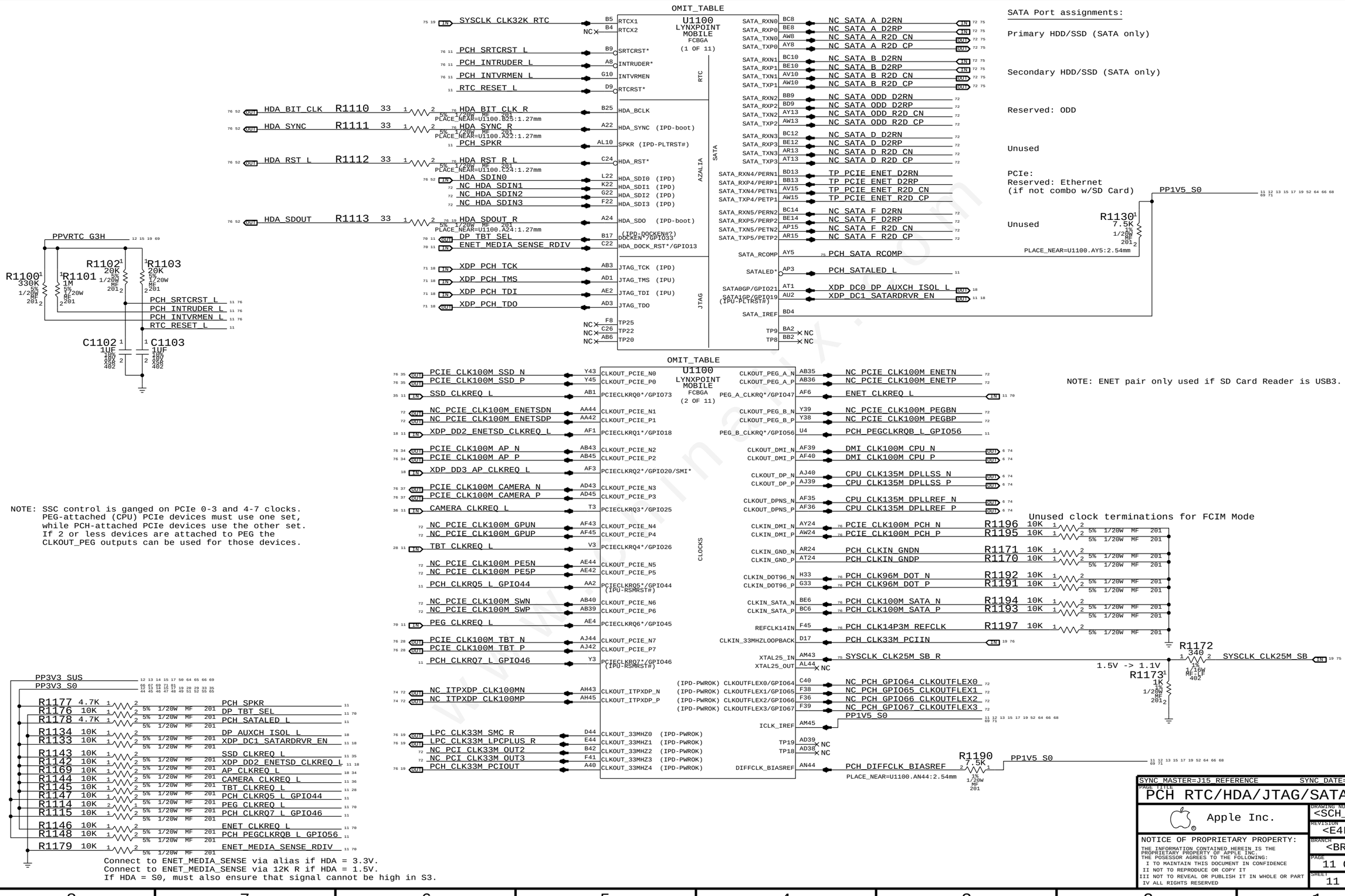

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OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (4 OF 11)

DMI_RXN0 AW22 ← DMI_N2S_N<0> (74 5 IN)
DMI_RXN1 AR20 ← DMI_N2S_N<1> (74 72 5 IN)
DMI_RXN2 AP17 ← DMI_N2S_N<2> (74 72 5 IN)
DMI_RXN3 AV20 ← DMI_N2S_N<3> (74 72 5 IN)
DMI_RXP0 AY22 ← DMI_N2S_P<0> (74 5 IN)
DMI_RXP1 AP20 ← DMI_N2S_P<1> (74 72 5 IN)
DMI_RXP2 AR17 ← DMI_N2S_P<2> (74 72 5 IN)
DMI_RXP3 AW20 ← DMI_N2S_P<3> (74 72 5 IN)
DMI_TXN0 BD21 → DMI_S2N_N<0> (74 5 OUT)
DMI_TXN1 BE20 → DMI_S2N_N<1> (74 72 5 OUT)
DMI_TXN2 BD17 → DMI_S2N_N<2> (74 72 5 OUT)
DMI_TXN3 BE18 → DMI_S2N_N<3> (74 72 5 OUT)
DMI_TXP0 BB21 → DMI_S2N_P<0> (74 5 OUT)
DMI_TXP1 BC20 → DMI_S2N_P<1> (74 72 5 OUT)
DMI_TXP2 BB17 → DMI_S2N_P<2> (74 72 5 OUT)
DMI_TXP3 BC18 → DMI_S2N_P<3> (74 72 5 OUT)

DMI / FDI

FDI_RXN0 AJ35 → NC
FDI_RXN1 AL35 → NC
FDI_RXP0 AJ36 → NC
FDI_RXP1 AL36 → NC
TP16 AV43 → NC
TP5 AY45 → NC
TP15 AV45 → NC
TP10 AW44 → NC
FDI_CSYNC AL39 ← FDI_CSYNC (OUT 5 74)
FDI_INT AL40 ← FDI_INT (OUT 5 74)
FDI_IREF AT45 ← R1210 1 7.5K 1% 1/20W MF 201 2 ← PP1V5_S0 (11 12 13 15 17 19 52 64 66 68 69 71)
PLACE_NEAR=U1100.AT45:12.7mm
R1215 1 330K 5% 1/20W MF 201 2 ← PPVRTC_G3H (11 15 19 69)
TP17 AU42 → NC
TP13 AU44 → NC
FDI_RCOMPO AR44 ← PCH_FDI_RCOMP

BE16 ← DMI_IREF
R1200 1 7.5K 1% 1/20W MF 201 2 ← PP1V5_S0 (68 66 64 52 19 17 15 13 12 11 71 69)
PLACE_NEAR=U1100.AY17:12.7mm
NC AW17 → TP12
NC AV17 → TP7
DMI_RCOMPO AY17 ← PCH_DMI_RCOMP

SYSTEM POWER MANAGEMENT

SUSACK* (IPU) R6 ← PCH_SUSACK_L
SYS_RESET* AM1 ← PM_SYSRST_L (76 71 41 19 IN)
SYS_PWROK AD7 ← PM_PCH_SYS_PWROK (76 71 41 19 18 IN)
PWROK F10 ← PM_PCH_PWROK (76 71 19 12 IN)
APWROK AB7 ← PM_PCH_PWROK (76 71 19 12 IN)
DRAMPWROK (OD) H3 ← PM_MEM_PWRGD (74 21 6 OUT)
RSMRST* J2 ← PM_RSMRST_L (76 71 66 IN)
SUSWARN*/SUSPWRNACK/GPIO30 J4 ← PCH_SUSWARN_L
PWRBTN* (IPU) K1 ← PM_PWRBTN_L (76 41 18 12 IN)
ACPRESENT/GPIO31 (IPD-DeepSx) E6 ← SMC_ADAPTER_EN (42 41 IN)
BATLOW*/GPIO72 K7 ← PM_BATLOW_L (43 41 30 12 IN)
RI* N4 ← PCH_RI_L
TP21 AB10 → TP_PCH_SLP_S0_L
SLP_WLAN*/GPIO29 D2 ← TP_PCH_SLP_WLAN_L

R1286 1 0 5% 1/20W MF 0201 2 ← PP3V3_SUS (69 66 65 64 50 17 15 14 13 11)
R1205 1 10K 5% 1/20W MF 201 2 ← PP3V3_SUS

DSWVRMEN C8 → PCH_DSWVRMEN (76)
DPWROK L13 ← PM_DSW_PWRGD (IN 41 71 76)
WAKE* (IPD-DeepSx) K3 → PCIE_WAKE_L (IN 12 34 36 71 76)
CLKRUN* AN7 ↔ PM_CLKRUN_L (BI 12 41 50 71)
SUS_STAT*/GPIO61 U7 → LPC_PWRDWN_L (OUT 20 41 50 71)
SUSCLK/GPIO62 (IPU-RSMRST#) Y6 → PM_CLK32K_SUSCLK_R (OUT 42)
SLP_S5*/GPIO63 Y7 → PM_SLP_S5_L (OUT 12 41 66)
SLP_S4* C6 → PM_SLP_S4_L (OUT 12 21 34 38 41 66 68 71)
SLP_S3* H1 → PM_SLP_S3_L (OUT 12 21 41 66 71)
SLP_A* F3 → TP_PM_SLP_A_L
SLP_SUS* F1 → PM_SLP_SUS_L (OUT 12 45 65 66)
PMSYNCH AY3 ← PM_SYNC (OUT 6 74)
SLP_LAN* G5 → TP_PCH_SLP_LAN_L

R1209 1 100K 5% 1/20W MF 201 2

OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (5 OF 11)

VGA_BLUE T45 → NC
VGA_GREEN U44 → NC
VGA_RED V45 → NC
VGA_DDC_CLK M43 → NC
VGA_DDC_DATA M45 → NC
VGA_HSYNC N42 → NC
VGA_VSYNC N44 → NC
DAC_IREF U40 → NC
VGA_IRTN U39 → NC

VGA DAC Disabled per SB DG v1.0 (Table 12-18).

CRT / DISPLAY / EDP

DDPB_CTRLCLK R40 → DP_TBTSNK0_DDC_CLK (33 70)
DDPB_CTRLDATA (IPD-PLTRST#) R39 → DP_TBTSNK0_DDC_DATA (33 70)
DDPC_CTRLCLK R35 → DP_TBTSNK1_DDC_CLK (33 70)
DDPC_CTRLDATA (IPD-PLTRST#) R36 → DP_TBTSNK1_DDC_DATA (33 70)
DDPD_CTRLCLK N40 → HDMI_DDC_CLK (68 70 71)
DDPD_CTRLDATA (IPD-PLTRST#) N38 → HDMI_DDC_DATA (68 70 71)
DDPB_AUXN H45 → DP_TBTSNK0_AUXCH_C_N (28 70 74)
DDPC_AUXN K43 → DP_TBTSNK1_AUXCH_C_N (28 70 74)
DDPD_AUXN J42 → NC_DP_IG_D_AUXCHN (72)
DDPB_AUXP H43 → DP_TBTSNK0_AUXCH_C_P (28 70 74)
DDPC_AUXP K45 → DP_TBTSNK1_AUXCH_C_P (28 70 74)
DDPD_AUXP J44 → NC_DP_IG_D_AUXCHP (72)
DDPB_HPD K40 → DP_TBTSNK0_HPD (28 70)
DDPC_HPD K38 → DP_TBTSNK1_HPD (28 70)
DDPD_HPD H39 → HDMI_HPD (20 68 70)

EDP_BKLTCTL N36 ← EDP_IG_BKL_PWM (70 63 OUT)
EDP_BKLTEN K36 ← EDP_IG_BKL_ON (71 70 63 12 OUT)
EDP_VDDEN G36 ← EDP_IG_PANEL_PWR (71 70 67 12 OUT)

PCI

PIRQA* H20 ← PCI_INTA_L
PIRQB* L20 ← PCI_INTB_L
PIRQC* K17 ← PCI_INTC_L
PIRQD* M20 ← PCI_INTD_L
GPIO50 A12 ← ENET_LOW_PWR_PCH (70 12 OUT)
GPIO52 B13 ← AUD_IPHS_SWITCH_EN_PCH (70 12 OUT)
GPIO54 C12 ← BT_PWRRST_L (70 12 OUT)
GPIO51 C10 ← TP_PCH_STRP_BBS1
GPIO53 A10 ← TP_PCH_STRP_ESI_L
GPIO55 AL6 ← PCH_STRP_TOPBLK_SWP_L (43 IN)
(IPU-PWROK&PCIRST#)

PIRQE*/GPIO2 G17 → SDCONN_OC_L (IN 12 70)
PIRQF*/GPIO3 F17 → AUD_IP_PERIPHERAL_DET (IN 12 70)
PIRQG*/GPIO4 L15 → TBT_PWR_REQ_L (IN 12 29)
PIRQH*/GPIO5 M15 → AUD_I2C_INT_L (IN 12 70)
(IPU) PME* AD10 → NC_PCI_PME_L (72)
PLTRST* Y11 → PLT_RESET_L (OUT 18 20 21 71)

R1260 10K 1 2 5% 1/20W MF 201 ← PCI_INTA_L
R1261 10K 1 2 5% 1/20W MF 201 ← PCI_INTB_L
R1262 10K 1 2 5% 1/20W MF 201 ← PCI_INTC_L
R1263 10K 1 2 5% 1/20W MF 201 ← PCI_INTD_L
PP3V3_S0 (33 29 20 19 81 71 69 67 66 65 55 52 51 49 48 47 46 45 44 35)

PP3V3_S5 (70 71 83 18 18 17 18 19 21 31 32 34 61)
PP3V3_S0 (65 66 67 69 71 81 84 65 66 69 35 44 46 46 47 48 49 51 52 56)

R1239 3.0K 5% 1/20W MF 201 ← PM_PWRBTN_L (12 18 41 76)
R1240 10K 5% 1/20W MF 201 ← PM_BATLOW_L (12 30 41 43)
R1291 10K 5% 1/20W MF 201 ← PM_CLKRUN_L (12 41 50 71)
R1216 10K 5% 1/20W MF 201 ← ENET_LOW_PWR_PCH (12 70)
R1217 100K 5% 1/20W MF 201 ← AUD_IPHS_SWITCH_EN_PCH (12 70)
R1218 10K 5% 1/20W MF 201 ← BT_PWRRST_L (12 70)
R1230 10K 5% 1/20W MF 201 ← SDCONN_OC_L (12 70)
NO STUFF Redundant to pull-up on audio page
R1214 100K 5% 1/20W MF 201 ← AUD_IP_PERIPHERAL_DET (12 70)
R1231 10K 5% 1/20W MF 201 ← TBT_PWR_REQ_L (12 29)
NO STUFF Redundant to pull-up on audio page
R1233 10K 5% 1/20W MF 201 ← AUD_I2C_INT_L (12 70)
R1225 1K 5% 1/20W MF 201 ← PCIE_WAKE_L (12 34 36 71 76)
R1224 100K 5% 1/20W MF 201 ← PM_SLP_S3_L (12 21 41 66 71)
R1221 100K 5% 1/20W MF 201 ← PM_SLP_S4_L (12 21 34 38 41 66 68 71)
R1222 100K 5% 1/20W MF 201 ← PM_SLP_S5_L (12 41 66)
R1223 100K 5% 1/20W MF 201 ← PM_SLP_SUS_L (12 45 65 66)
R1281 100K 5% 1/20W MF 201 ← EDP_IG_BKL_ON (12 63 70 71)
R1284 100K 5% 1/20W MF 201 ← EDP_IG_PANEL_PWR (12 67 70 71)

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: PCH DMI/FDI/PM/GFX/PCI

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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USB3 Port Assignments:

Unused

PCIe/USB3 Port Assignments:

SD Card Reader
(& Ethernet if combo)

PCIe Port Assignments:

AirPort

Camera

SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(9 OF 11)

PCI-E

NC_USB3_SPARE_D2RN — AW31 PERN1_USB3RN3
NC_USB3_SPARE_D2RP — AY31 PERP1_USB3RP3
NC_USB3_SPARE_R2D_CN — BE32 PETN1_USB3TN3
NC_USB3_SPARE_R2D_CP — BC32 PETP1_USB3TP3

USB3_SD_D2R_N — AT31 PERN2_USB3RN4
USB3_SD_D2R_P — AR31 PERP2_USB3RP4
USB3_SD_R2D_C_N — BD33 PETN2_USB3TN4
USB3_SD_R2D_C_P — BB33 PETP2_USB3TP4

PCIE_AP_D2R_N — AW33 PERN3
PCIE_AP_D2R_P — AY33 PERP3
PCIE_AP_R2D_C_N — BE34 PETN3
PCIE_AP_R2D_C_P — BC34 PETP3

PCIE_CAMERA_D2R_N — AT33 PERN4
PCIE_CAMERA_D2R_P — AR33 PERP4
PCIE_CAMERA_R2D_C_N — BE36 PETN4
PCIE_CAMERA_R2D_C_P — BC36 PETP4

PCIE_SSD_D2R_N<0> — AW36 PERN5
PCIE_SSD_D2R_P<0> — AV36 PERP5
PCIE_SSD_R2D_C_N<0> — BD37 PETN5
PCIE_SSD_R2D_C_P<0> — BB37 PETP5

PCIE_SSD_D2R_N<1> — AY38 PERN6
PCIE_SSD_D2R_P<1> — AW38 PERP6
PCIE_SSD_R2D_C_N<1> — BC38 PETN6
PCIE_SSD_R2D_C_P<1> — BE38 PETP6

PCIE_SSD_D2R_N<2> — AT40 PERN7
PCIE_SSD_D2R_P<2> — AT39 PERP7
PCIE_SSD_R2D_C_N<2> — BE40 PETN7
PCIE_SSD_R2D_C_P<2> — BC40 PETP7

PCIE_SSD_D2R_N<3> — AN38 PERN8
PCIE_SSD_D2R_P<3> — AN39 PERP8
PCIE_SSD_R2D_C_N<3> — BD42 PETN8
PCIE_SSD_R2D_C_P<3> — BD41 PETP8

PP1V5_S0
R1300 7.5K 1% 1/20W MF 201 — PLACE_NEAR=U1100.BD29:12.7mm
PCH_PCIE_RCOMP — BD29 PCIE_RCOMP
BE30 PCIE_IREF
NC — BC30 TP11
NC — BB29 TP6

USB

USB2N0 B37 USB_EXTA_N
USB2P0 D37 USB_EXTA_P
USB2N1 A38 NC_USB_EXTCN
USB2P1 C38 NC_USB_EXTCP
USB2N2 A36 NC_USB_SDN
USB2P2 C36 NC_USB_SDP
USB2N3 A34 NC_USB_WLANN
USB2P3 C34 NC_USB_WLANP
USB2N4 B33 NC_USB_4N
USB2P4 D33 NC_USB_4P
USB2N5 F31 NC_USB_PSOCN
USB2P5 G31 NC_USB_PSOCP
USB2N6 K31 NC_USB_6N
USB2P6 L31 NC_USB_6P
USB2N7 G29 NC_USB_7N
USB2P7 H29 NC_USB_7P
USB2N8 A32 USB_EXTB_N
USB2P8 C32 USB_EXTB_P
USB2N9 A30 NC_USB_EXTDN
USB2P9 C30 NC_USB_EXTDP
USB2N10 B29 TP_USB_CAMERAN
USB2P10 D29 TP_USB_CAMERAP
USB2N11 A28 USB_BT_N
USB2P11 C28 USB_BT_P
USB2N12 G26 NC_USB_IRN
USB2P12 F26 NC_USB_IRP
USB2N13 F24 USB_TPAD_N
USB2P13 G24 USB_TPAD_P
(IPD)

USB3RN1 AR26 USB3_EXTA_D2R_N
USB3RP1 AP26 USB3_EXTA_D2R_P
USB3TN1 BE24 USB3_EXTA_R2D_C_N
USB3TP1 BD23 USB3_EXTA_R2D_C_P
USB3RN2 AW26 USB3_EXTB_D2R_N
USB3RP2 AV26 USB3_EXTB_D2R_P
USB3TN2 BD25 USB3_EXTB_R2D_C_N
USB3TP2 BC24 USB3_EXTB_R2D_C_P
USB3RN5 AW29 NC_USB3_EXTC_D2RN
USB3RP5 AV29 NC_USB3_EXTC_D2RP
USB3TN5 BE26 NC_USB3_EXTC_R2D_CN
USB3TP5 BC26 NC_USB3_EXTC_R2D_CP
USB3RN6 AR29 NC_USB3_EXTD_D2RN
USB3RP6 AP29 NC_USB3_EXTD_D2RP
USB3TN6 BD27 NC_USB3_EXTD_R2D_CN
USB3TP6 BE28 NC_USB3_EXTD_R2D_CP

USBRBIAS* K24
USBRBIAS K26
PCH_USB_RBIAS
R1370 22.6 1% 1/20W MF 201 — PLACE_NEAR=U1100.K24:11.4mm

TP24 M33 NC
TP23 L33 NC

OC0*/GPIO59 P3 XDP_DA0_USB_EXTA_OC_L
OC1*/GPIO40 V1 XDP_DA1_USB_EXTC_OC_L
OC2*/GPIO41 U2 XDP_DA2_SSD_PWR_EN
OC3*/GPIO42 P1 XDP_DA3_CAMERA_PWR_EN
OC4*/GPIO43 M3 XDP_DB0_USB_EXTB_OC_L
OC5*/GPIO9 T1 XDP_DB1_USB_EXTD_OC_L
OC6*/GPIO16 N2 XDP_DB2_SD_PWR_EN
OC7*/GPIO14 M1 XDP_DB3_SDCONN_STATE_CHANGE_L

USB Port Assignments:

Ext A (LS/FS/HS)

Ext C (LS/FS/HS)

Reserved: SD (HS)

Reserved: WiFi (HS)

Unused

Reserved: PSOC (Legacy Trackpad)

Unused

Unused

Ext B (LS/FS/HS)

Ext D (LS/FS/HS)

Reserved: Camera

BT

IR

Trackpad

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

Ext C (SS)

Ext D (SS)

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(3 OF 11)

LPC_AD<0> — R1340 33 — LPC_AD_R<0> — A20 LAD0 (IPU)
LPC_AD<1> — R1341 33 — LPC_AD_R<1> — C20 LAD1 (IPU)
LPC_AD<2> — R1342 33 — LPC_AD_R<2> — A18 LAD2 (IPU)
LPC_AD<3> — R1343 33 — LPC_AD_R<3> — C18 LAD3 (IPU)
LPC_FRAME_L — R1344 33 — LPC_FRAME_R_L — B21 LFRAME*
NC_LPC_DREQ0_L — D21 LDRQ0* (IPU)
TBT_PWR_EN_PCH — G20 LDRQ1*/GPIO23 (IPU-LDRQ1#?)
LPC_SERIRQ — AL11 SERIRQ

LPC

SPI_CLK_R — AJ11 SPI_CLK
SPI_CS0_R_L — AJ7 SPI_CS0* (IPU)
TP_SPI_CS1_L — AL7 SPI_CS1* (IPU)
TP_SPI_CS2_L — AJ10 SPI_CS2* (IPU)
SPI_MOSI_R — AH1 SPI_MOSI (IPD)
SPI_MISO — AH3 SPI_MISO (IPU)
SPI_IO<2> — AJ4 SPI_IO2 (IPU)
SPI_IO<3> — AJ2 SPI_IO3 (IPU)

SPI

SMBUS

SMBALERT*/GPIO11 — N7 — PCH_SMBALERT_L
SMBCLK — R10 — SMBUS_PCH_CLK
SMBDATA — U11 — SMBUS_PCH_DATA
SML0ALERT*/GPIO60 — N8 — PCH_SML0ALERT_L
SML0CLK — U8 — SML_PCH_0_CLK
SML0DATA — R7 — SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO74 — H6 — PCH_SML1ALERT_L
SML1CLK/GPIO58 — K6 — SML_PCH_1_CLK
SML1DATA/GPIO75 — N11 — SML_PCH_1_DATA

C-LINK

(IPU/IPD) CL_CLK — AF11 — NC_CLINK_CLK
(IPU/IPD) CL_DATA — AF10 — NC_CLINK_DATA
CL_RST* — AF7 — NC_CLINK_RESET_L

TP1 BA45 NC
TP2 BC45 NC
TP4 BE43 NC
TP3 BE44 NC
TD_IREF — AY43 — PCH_TD_IREF
R1380 9.2K 1% 1/20W MF 201

PP3V3_SUS
PP3V3_SUS
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0

R1350 10K — LPC_SERIRQ
R1351 10K — TBT_PWR_EN_PCH
R1360 10K — XDP_DA0_USB_EXTA_OC_L
R1361 10K — XDP_DA1_USB_EXTC_OC_L
R1362 10K — SSD_PWR_EN
R1368 10K — CAMERA_PWR_EN
R1320 10K — XDP_DB0_USB_EXTB_OC_L
R1321 10K — XDP_DB1_USB_EXTD_OC_L
R1367 10K — SD_PWR_EN
R1369 10K — XDP_DB3_SDCONN_STATE_CHANGE_L
R1392 1K — SPI_IO<2>
R1393 1K — SPI_IO<3>
R1353 10K — PCH_SMBALERT_L
R1354 10K — PCH_SML0ALERT_L
R1355 10K — PCH_SML1ALERT_L

5% 1/20W MF 201

SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012

PAGE TITLE
PCH PCI-E/USB

Apple Inc.

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Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(6 OF 11)

CPU/MISC
GPIO

TBT_CIO_PLUG_EVENT_L — AT8 BMBUSY*/GPIO0
FW_PME_L — F13 TACH1/GPIO1
DPMUX_UC_IRQ — A14 TACH2/GPIO6
SMC_RUNTIME_SCI_L — G15 TACH3/GPIO7
XDP_FC0_HDD_PWR_EN — Y1 GPIO8 (IPU-RSMRST#)
WOL_EN — K13 LAN_PHY_PWR_CTRL/GPIO12
MEM_VDD_SEL_1V5_L — AB11 GPIO15
XDP_DD0_SSD_PCIE_SEL_L — AN2 SATA4GP/GPIO16 (IPU-BOOT/SATA4GP?)
LPCPLUS_GPIO — C14 TACH0/GPIO17
JTAG_TBT_TMS_PCH — BB4 SCLOCK/GPIO22
TBT_GO2SX_BIDIR — Y10 GPIO24
SMC_WAKE_SCI_L — R11 GPIO27 (IPU-DeepSx)
ISOLATE_CPU_MEM_L — AD11 GPIO28
TBT_POC_RESET_L — AN6 GPIO34
XDP_FC1_GPU_GOOD — AP1 GPIO35/NMI*
XDP_DC2_ODD_PWR_EN_L — AT3 SATA2GP/GPIO36 (IPD-PLTRST#)
XDP_DC3_JTAG_ISP_TCK — AK1 SATA3GP/GPIO37 (IPD-PLTRST#)
JTAG_ISP_TDO — AT7 SLOAD/GPIO38
JTAG_ISP_TDI — AM3 SDATAOUT0/GPIO39
FW_PWR_EN_PCH — AN4 SDATAOUT1/GPIO48
XDP_DD1_MLB_RAMCFG1 — AK3 SATA5GP/GPIO49 (IPU-BOOt/SATA5GP?)
SPIROM_USE_MLB — U12 GPIO57
MLB_RAMCFG3 — C16 TACH4/GPIO68
MLB_RAMCFG2 — D13 TACH5/GPIO69
SD_SEL_PCIE_L_USB_H — G13 TACH6/GPIO70 (IPU-BOot?)
MLB_RAMCFG0 — H15 TACH7/GPIO71 (IPU-BOot?)

BE41, BE5, C45, A5 — VSS

TP14 — AN10 — PCH_A20GATE
(IPD) PECI — AY1 — PCH_PECI
RCIN* — AT6 — PCH_RCIN_L
PROCPWRGD — AV3 — PCH_PROCPWRGD
THRMTRIP* — AV1 — PM_THRMTRIP_L_R
PLTRST_PROC* — AU4 — CPU_RESET_L
VSS — N10

A2, A41, A43, A44, B1, B2, B44, B45, BA1, BC1, BD1, BD2, BD44, BD45, BE2, BE3, D1, E1, E45, A4 — VSS

PP1V05_S0
NO STUFF
R1457 1K 5% 1/16W MF-LF 402

PCH_A20GATE — 14
PCH_PECI — R1470 43 — CPU_PECI
PCH_RCIN_L — 14 76
PCH_PROCPWRGD — R1440 0 — CPU_PWRGD
PM_THRMTRIP_L_R — R1456 390 — PM_THRMTRIP_L
CPU_RESET_L

NO STUFF
R1470 43 5% 1/20W MF 201 — CPU_PECI
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L

PP3V3_S0
RAMCFG0:H R1475 10K 5% 1/20W MF 201
RAMCFG1:H R1474 10K 5% 1/20W MF 201
RAMCFG2:H R1473 10K 5% 1/20W MF 201
RAMCFG3:H R1472 10K 5% 1/20W MF 201

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PP3V3_S5
PP3V3_SUS
PP3V3_S0

NOTE: GPIO0 pull-up/down on project-specific page

R1485 10K — FW_PME_L
R1411 20K — DPMUX_UC_IRQ
R1496 10K — SMC_RUNTIME_SCI_L
R1494 10K — WOL_EN
R1489 10K — MEM_VDD_SEL_1V5_L
R1495 100K — XDP_DD0_SSD_PCIE_SEL_L
R1490 100K — LPCPLUS_GPIO
R1412 10K — JTAG_TBT_TMS_PCH
R1492 10K — TBT_GO2SX_BIDIR
R1491 10K — SMC_WAKE_SCI_L
R1498 10K — XDP_DC2_ODD_PWR_EN_L
R1413 10K — JTAG_ISP_TCK
R1486 10K — JTAG_ISP_TDO
R1499 10K — JTAG_ISP_TDI
R1484 10K — FW_PWR_EN_PCH
R1493 100K — SPIROM_USE_MLB

NOTE: GPIO70 pull-up/down on project-specific page

R1450 10K — PCH_A20GATE
R1455 10K — PCH_RCIN_L

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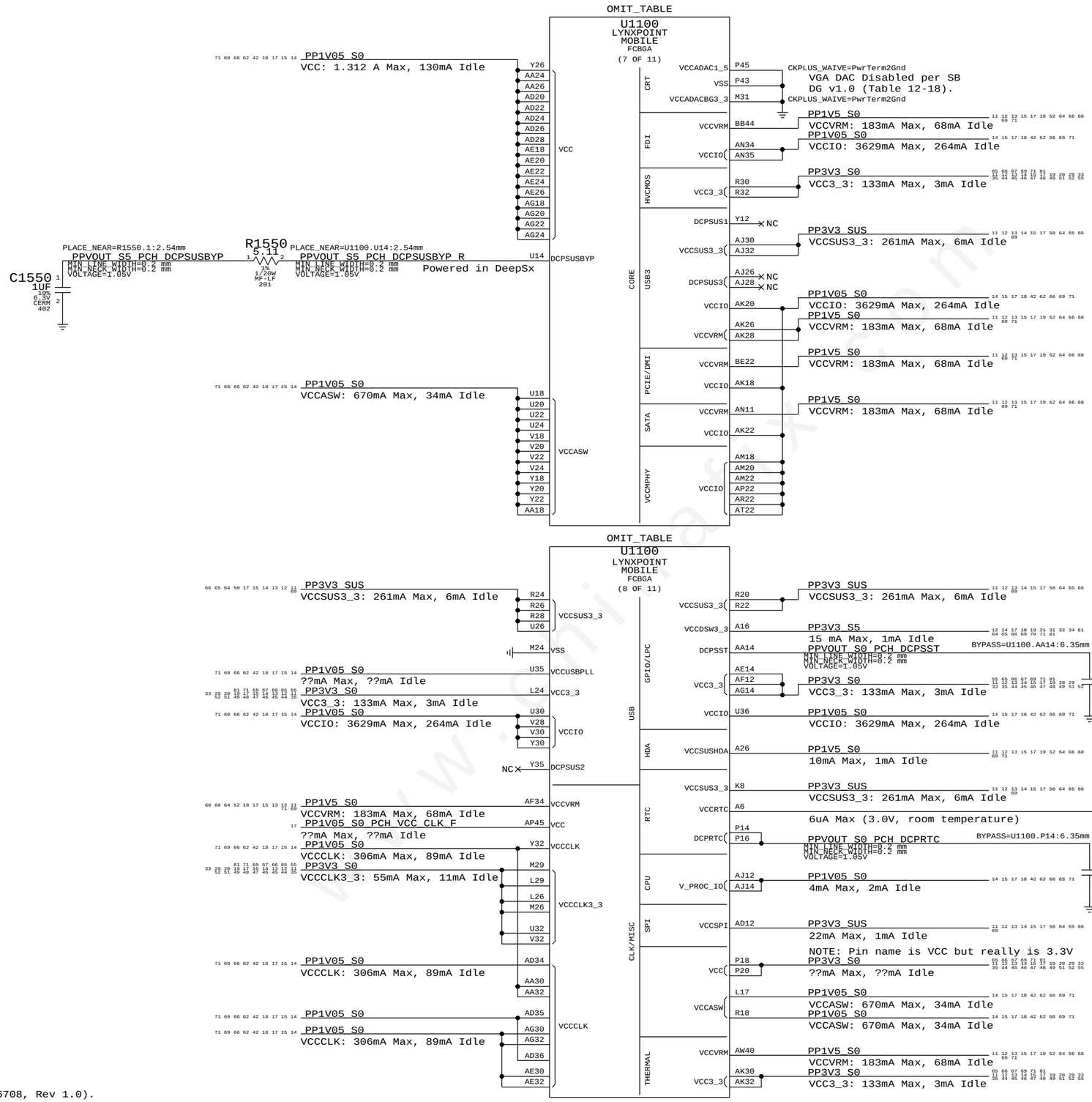

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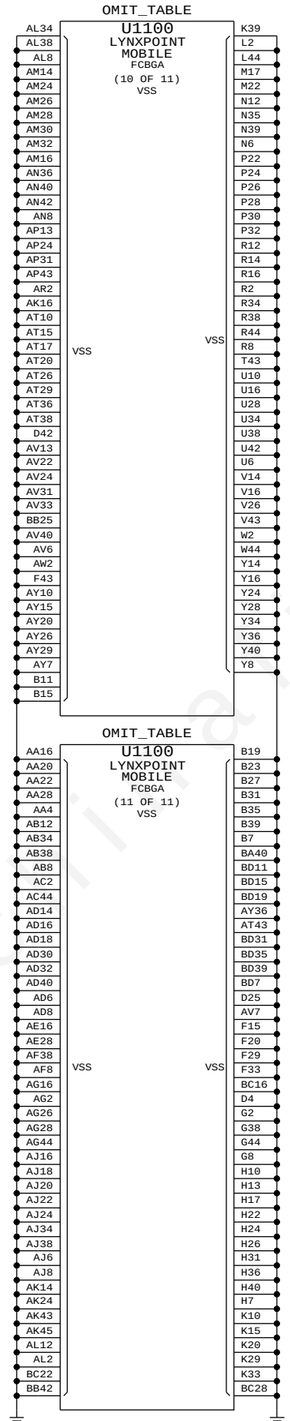

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PCH Grounds

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.A16:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD12:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1704 0.1UF 20% 10V CERM 402
BYPASS=U1100.R20:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS

C1706 0.1UF 20% 10V CERM 402
BYPASS=U1100.R26:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.K8:6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0

C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.L26:6.35mm
BYPASS=U1100.L29:6.35mm
BYPASS=U1100.M29:6.35mm
BYPASS=U1100.U32:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0

C1726 0.1UF 20% 10V CERM 402
BYPASS=U1100.R30:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0

C1730 0.1UF 20% 10V CERM 402
BYPASS=U1100.L24:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1732 0.1UF 20% 10V CERM 402
BYPASS=U1100.AK30:6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0

C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.P18:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle

C1750 22UF 20% 6.3V X5R-CERM-1 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1755 10UF 20% 6.3V X5R 603
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.AG18:12.7mm
BYPASS=U1100.AG22:6.35mm
BYPASS=U1100.AP20:6.35mm
BYPASS=U1100.AE18:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0

C1760 10UF 20% 6.3V X5R 603
C1761 1UF 10% 6.3V CERM 402
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.AK18:12.7mm
BYPASS=U1100.AG18:6.35mm
BYPASS=U1100.AK22:6.35mm
BYPASS=U1100.AP20:6.35mm
BYPASS=U1100.AM18:6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0

C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.U35:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0

C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.AN34:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1774 0.1UF 20% 10V CERM 402
BYPASS=U1100.U30:6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0

C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.AJ12:12.7mm
BYPASS=U1100.AJ12:6.35mm
BYPASS=U1100.AJ12:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0

C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AE30:6.35mm
BYPASS=U1100.AG30:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0

C1778 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD35:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0

C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD34:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0

C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA30:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0

C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.A26:6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

C1740 10UF 20% 6.3V X5R 603
BYPASS=U1100.AF34:12.7mm

PP1V05_S0
??mA Max, ??mA Idle

R1790 1 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT TABLE
L1790 4.7UH-170MA-0.321OHM 0603

PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V

NO STUFF
C1790 10UF 20% 6.3V X5R 603
C1791 1UF 10% 10V X5R 402
BYPASS=U1100.AP45:12.7mm
BYPASS=U1100.AP45:6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

PP1V05_S0 → R1830 150 5% 1/16W MF-LF 402 → CRITICAL XDP_CONN J1800 DF40RC-60DP-0.4V M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

XDP_CPU_PRESENT_L

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.F50:2.54mm)
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 (PLACE_NEAR=U5000.J3:2.54mm)
PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402

R1805 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.A67:2.54mm): PLT_RESET_L → XDP_PCH_TDO, XDP_PCH_TDI, XDP_PCH_TMS

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.51:28mm): XDP_CPU_TDO
CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.53:28mm): XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE)
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.55:28mm): XDP_CPU_TDI
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.57:28mm): XDP_CPU_TMS

R1820 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.M49:28mm): XDP_CPU_TDO
R1823 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.N54:28mm): XDP_CPU_TCK
R1824 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.M53:28mm): XDP_CPUPCH_TRST_L

TDI and TMS are terminated in CPU.

PCH/XDP Signals

OMIT (All 10 R's)

XDP_DA0_USB_EXTA_OC_L	R1890	SHORT	USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895	SHORT	SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893	SHORT	CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894	SHORT	USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896	SHORT	SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897	SHORT	SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872	SHORT	DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN	MAKE_BASE=TRUE		XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L	MAKE_BASE=TRUE		XDP_DC2_ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875	SHORT	JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876	SHORT	SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1	MAKE_BASE=TRUE		XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L	MAKE_BASE=TRUE		XDP_DD2_ENETSD_CLKREQ
XDP_DD3_AP_CLKREQ_L	R1879	SHORT	AP_CLKREQ_L

(NONE NONE NONE 201)

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

(TP-P6)

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD

C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, NC)
R1845 330K 5% 1/20W MF 201

XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

R1860 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AD3:28mm): XDP_PCH_TDO
R1861 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AE2:28mm): XDP_PCH_TDI
R1862 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AD1:28mm): XDP_PCH_TMS
R1866 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AB3:28mm): XDP_PCH_TCK

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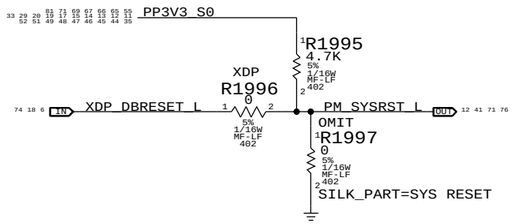
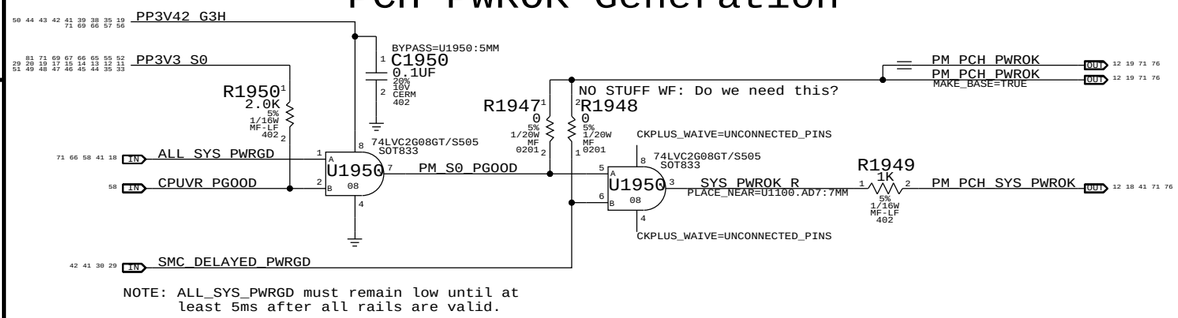
PCH Reset Button

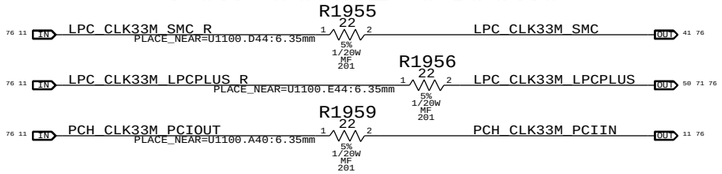


PCH PWROK Generation



NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

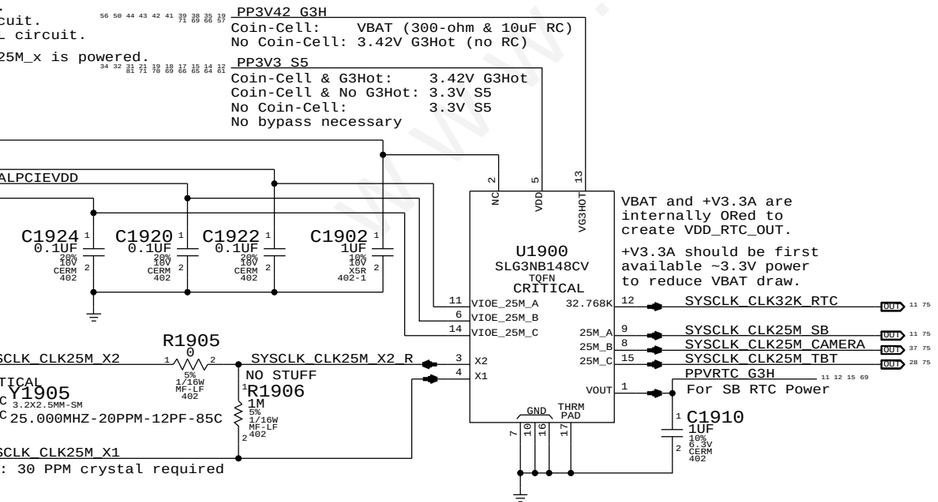
PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenClk 25MHz Power — PP3V3_S5

SB XTAL Power — PP1V5_S0
Camera XTAL Power — PP1V2_CAM_XTALPCIEVDD
TBT XTAL Power — PP3V3_TBTLC

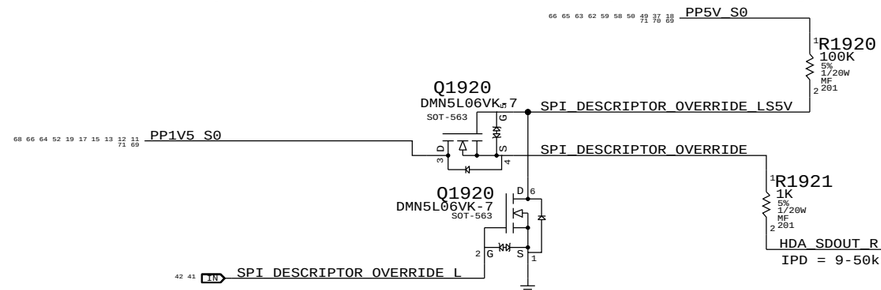
NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).



NOTE: 30 PPM crystal required

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



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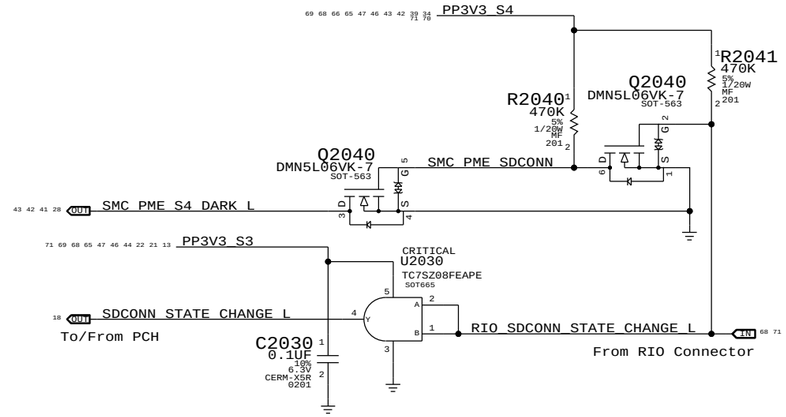
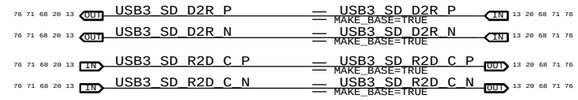
RIO SD Card Reader Support



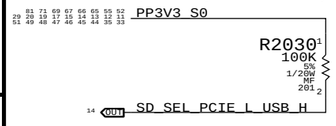
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



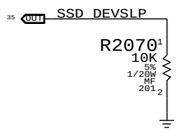
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe



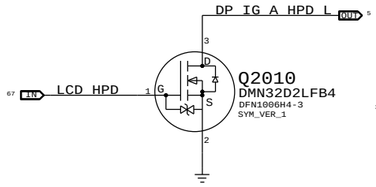
GS3 Connector Support

DEVSLP not supported on LPT-H

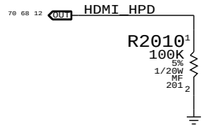


LCD HPD Inverter

(Pull-Up on CPU Page)

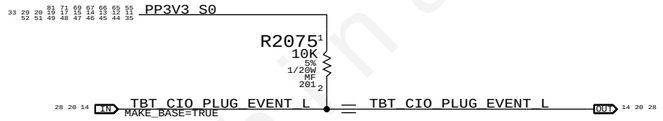


HDMI HPD pull-down



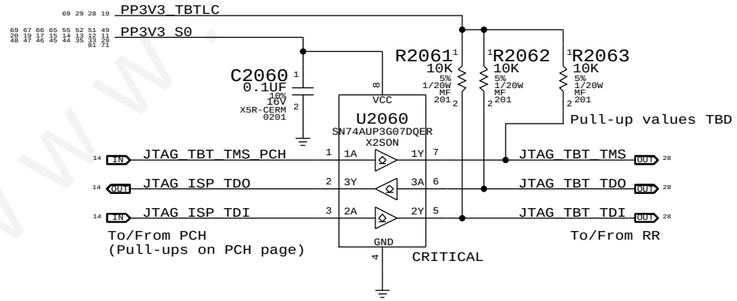
Redwood Ridge Support

RR output is open-drain, no isolation necessary

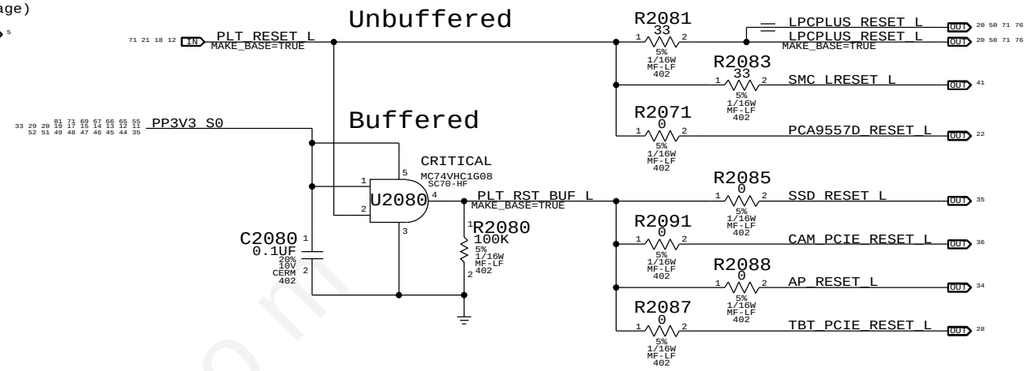


Redwood Ridge JTAG Isolation

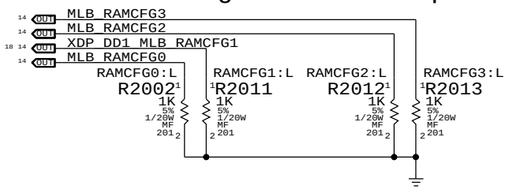
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



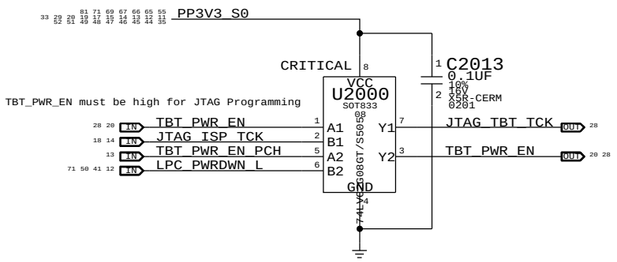
Platform Reset Connections



RAM Configuration Straps



GPIO Glitch Prevention



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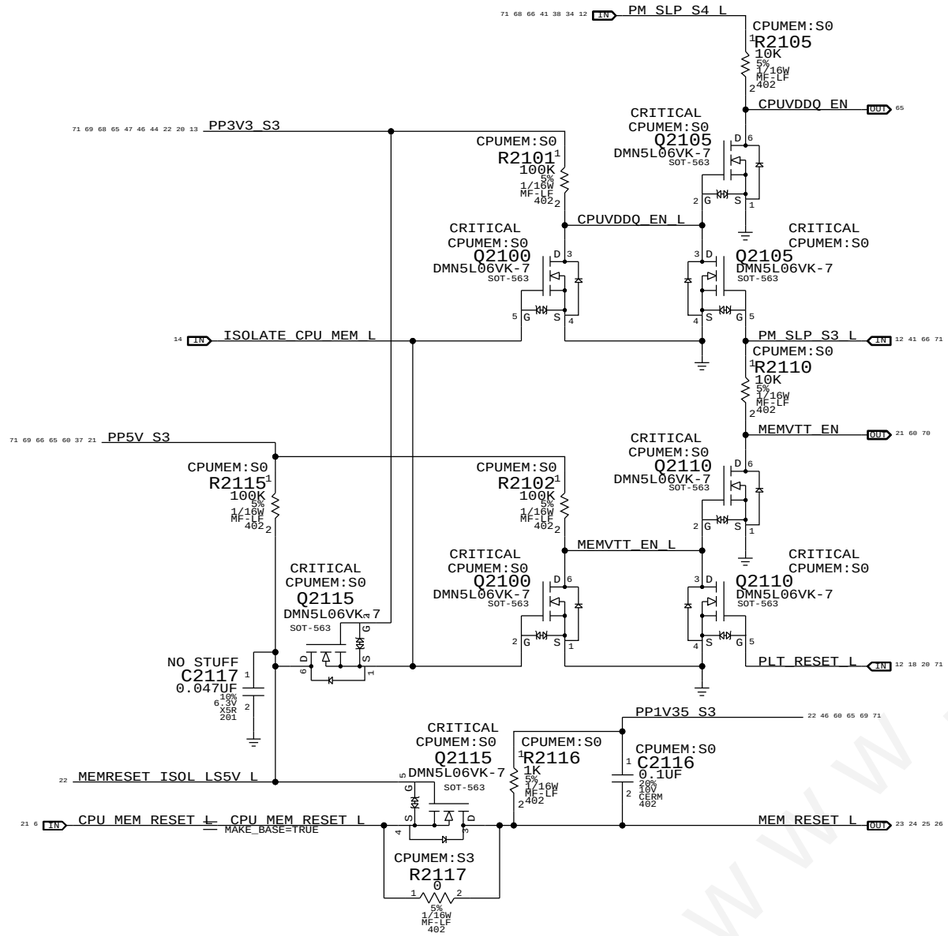
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



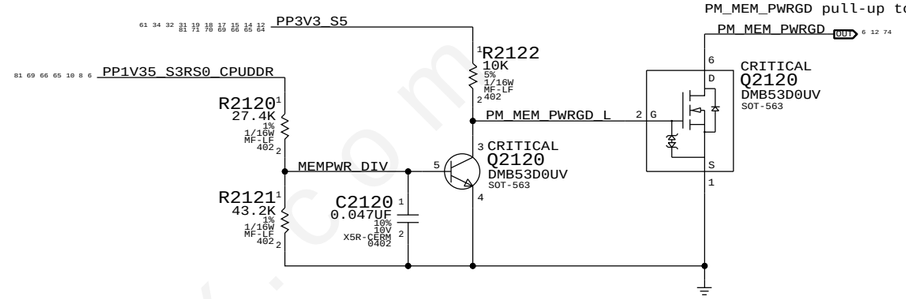
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

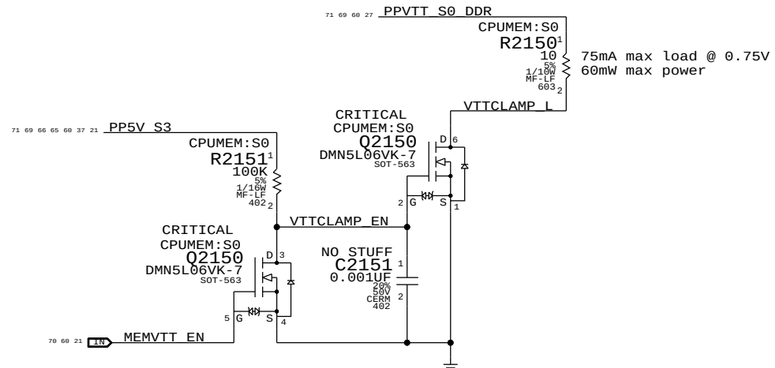
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

21 IN MEMRESET_ISOL_LS5V_L
74 7 IN CPU_DIMMA_VREFDQ
74 7 IN CPU_DIMMB_VREFDQ
7 IN CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

EN RC's to avoid drain glitches

DDRVREF_DAC R2225 100K 1% 1/10W MF-LF 402 — VREFMRGN_DQ_A_EN_RC — DDRVREF_DAC C2225 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2245 100K 1% 1/10W MF-LF 402 — VREFMRGN_DQ_B_EN_RC — DDRVREF_DAC C2245 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2265 100K 1% 1/10W MF-LF 402 — VREFMRGN_CA_A_EN_RC — DDRVREF_DAC C2265 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2285 100K 1% 1/10W MF-LF 402 — VREFMRGN_CA_B_EN_RC — DDRVREF_DAC C2285 0.1UF 20% 10V CERM 402

DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC R2208 100K 5% 1/20W MF 201

CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 — VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 — VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 — VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 — VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

PP1V35_S3 21 46 60 65 69 71

PLACE_NEAR=C2220.1:2mm
R2223 2 5% 1/20W MF 201
PLACE_NEAR=C2220.6:2mm
C2220 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFDQ_A_RC
PLACE_NEAR=R2221.2:1mm
R2222 1K 1% 1/16W MF-LF 402
R2220 24.9 1% 1/20W MF 201
PLACE_NEAR=R2223.2:1mm
PP0V75_S3_MEM_VREFDQ_A 23 24 70 74 77
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2240.1:2mm
R2243 2 5% 1/20W MF 201
PLACE_NEAR=Q2240.6:2mm
C2240 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFDQ_B_RC
PLACE_NEAR=R2241.2:1mm
R2242 1K 1% 1/16W MF-LF 402
R2240 24.9 1% 1/20W MF 201
PLACE_NEAR=R2243.2:1mm
PP0V75_S3_MEM_VREFDQ_B 23 26 70 74
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2260.1:2mm
R2263 2 5% 1/20W MF 201
PLACE_NEAR=Q2220.3:2mm
C2260 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFCA_A_RC
PLACE_NEAR=R2261.2:1mm
R2262 1K 1% 1/16W MF-LF 402
R2260 24.9 1% 1/20W MF 201
PLACE_NEAR=R2263.2:1mm
PP0V75_S3_MEM_VREFCA_A 23 24 70 74 77
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2280.1:2mm
R2283 2 5% 1/20W MF 201
PLACE_NEAR=Q2260.3:2mm
C2280 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFCA_B_RC
PLACE_NEAR=R2281.2:1mm
R2282 1K 1% 1/16W MF-LF 402
R2280 24.9 1% 1/20W MF 201
PLACE_NEAR=R2283.2:1mm
PP0V75_S3_MEM_VREFCA_B 25 26 70 74
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

R2221 1K 1% 1/16W MF-LF 402
R2241 1K 1% 1/16W MF-LF 402
R2261 1K 1% 1/16W MF-LF 402
R2281 1K 1% 1/16W MF-LF 402

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

47 46 44 22 21 20 18 13 PP3V3_S3
OMIT R2218 SHORT NONE NONE NONE NONE 402

PP3V3_S3_VREFMRGN
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2200 MSOP DAC5574
VDD 8
GND 3
SCL 6 — 44 22 18 13 76 71 68 63 IN SMBUS_PCH_CLK
SDA 7 — 44 22 18 13 76 71 68 63 BI SMBUS_PCH_DATA
A0 9
A1 10
Addr=0x98(WR)/0x99(RD)
VOUTA 1 — VREFMRGN_DQ_A
VOUTB 2 — VREFMRGN_DQ_B
VOUTC 4 — VREFMRGN_CA_AB
VOUTD 5 — VREFMRGN_MEMVREG_FBVREF

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2201 QFN PCA9557
VCC 16
A0 3
A1 4
A2 5
Addr=0x30(WR)/0x31(RD)
(OD) P0 6 — NC
P1 7 — VREFMRGN_DQ_A_EN
P2 9 — VREFMRGN_DQ_B_EN
P3 10 — VREFMRGN_CA_A_EN
P4 11 — VREFMRGN_CA_B_EN
P5 12 — VREFMRGN_MEMVREG_EN
P6 13 — VREFMRGN_FRAMEBUF_EN
P7 14 — NC
SCL 1 — 76 71 68 63 44 22 18 13 IN SMBUS_PCH_CLK
SDA 2 — 76 71 68 63 44 22 18 13 BI SMBUS_PCH_DATA
RESET* 15 — 20 IN PCA9557D_RESET_L
THRM PAD 17
GND 8

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PP3V3_S3 13 20 21 22 44 46 47 65 68 69 71
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
B3 V+ C2 C1 C4 B4 V- C3
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402 — DDRREG_FB OUT 60

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
A2 V+ B3 A1 A4 B4 V- A3
VREFMRGN_FRAMEBUF_BUF
DDRVREF_DAC R2217 1M 5% 1/16W MF-LF 402

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2215 100K 5% 1/20W MF 201

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

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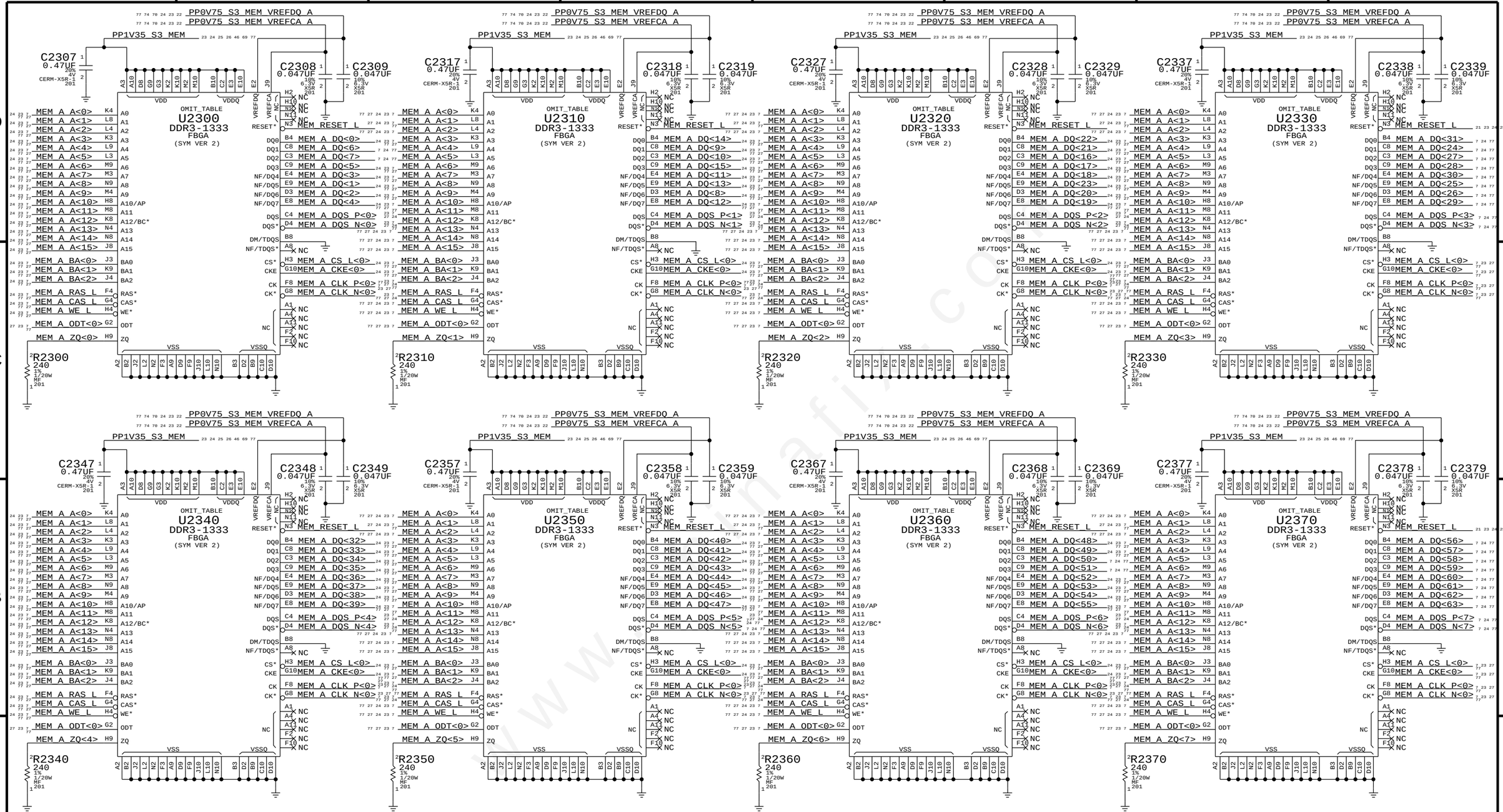

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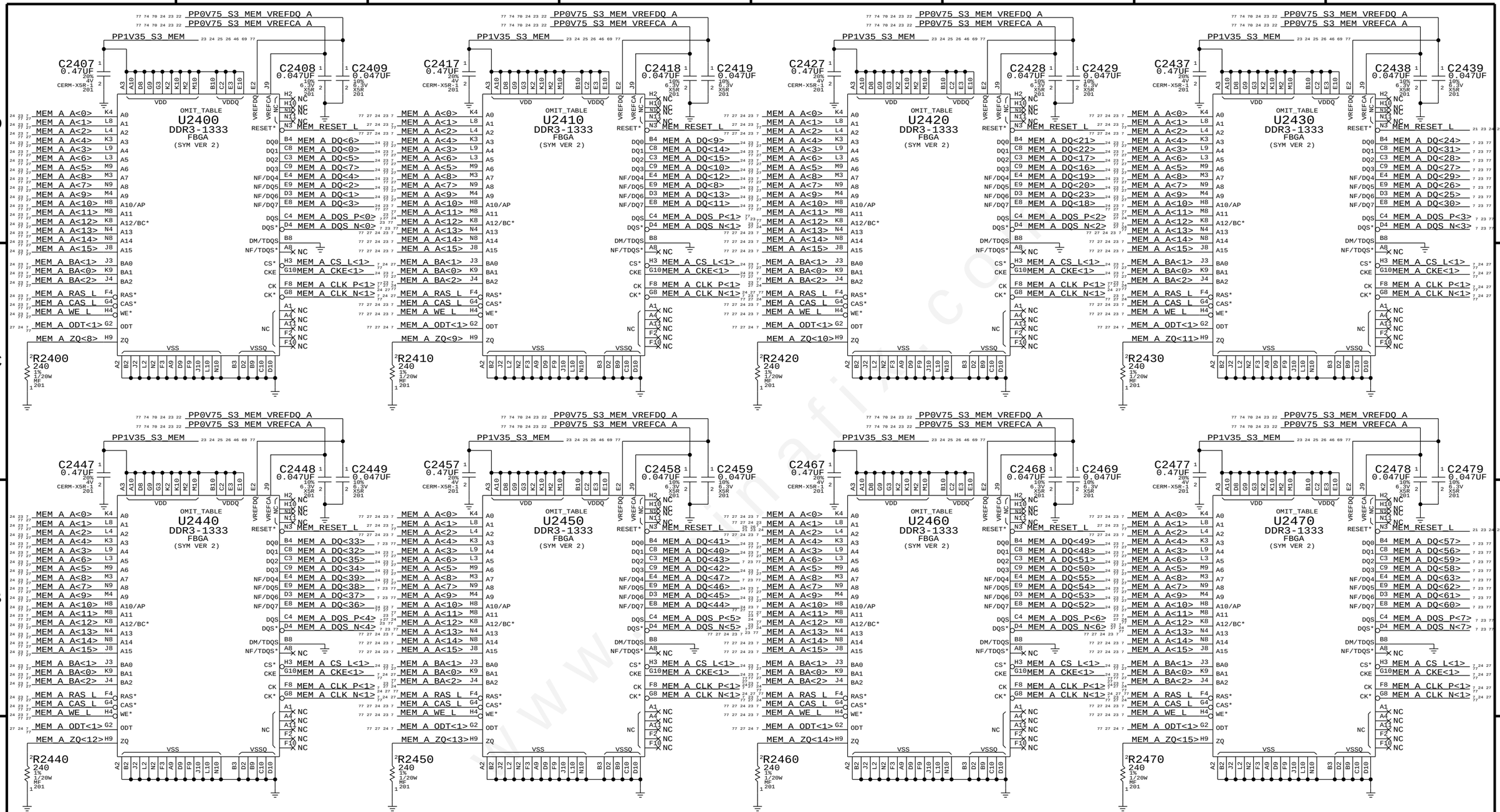

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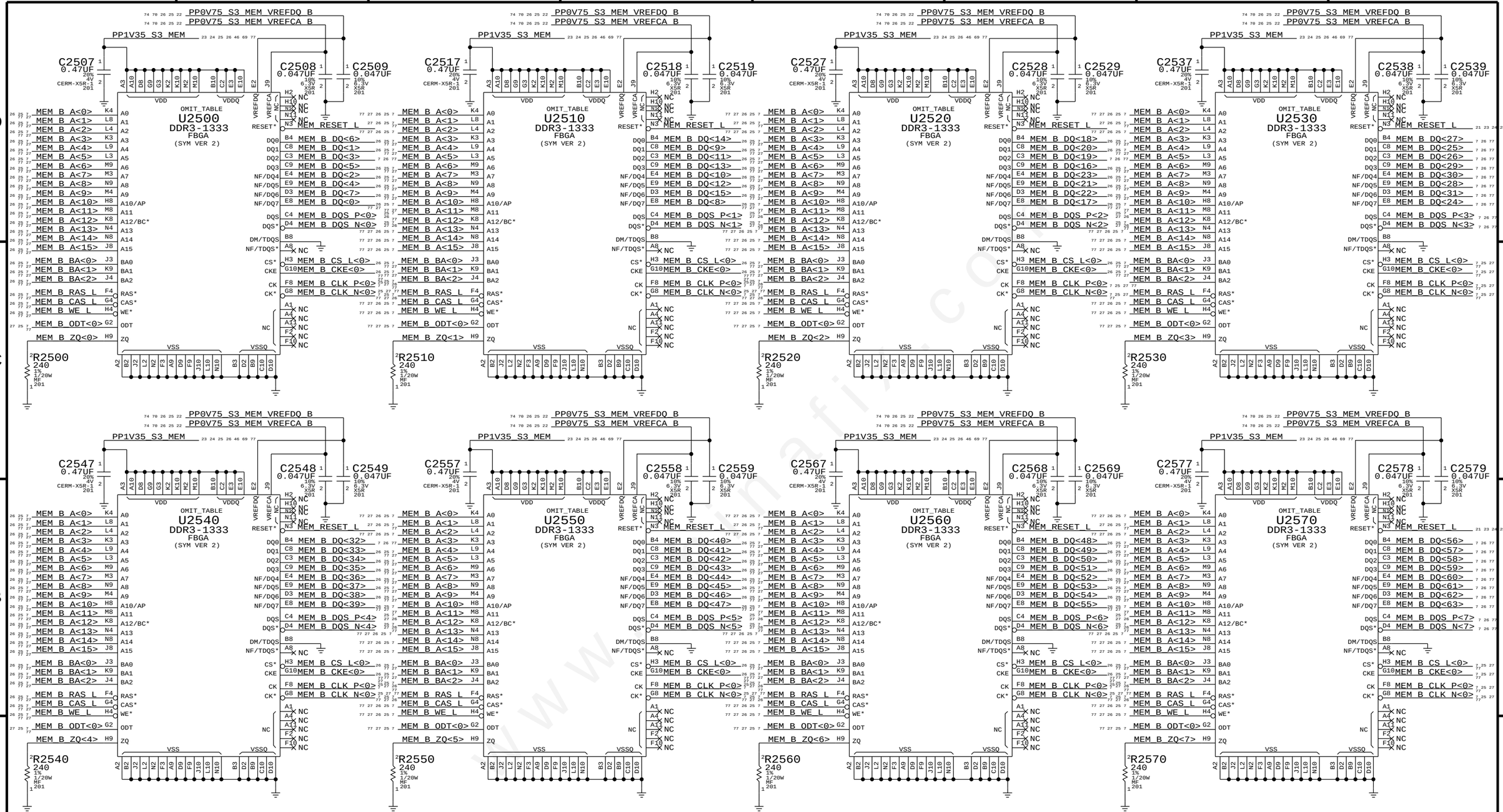

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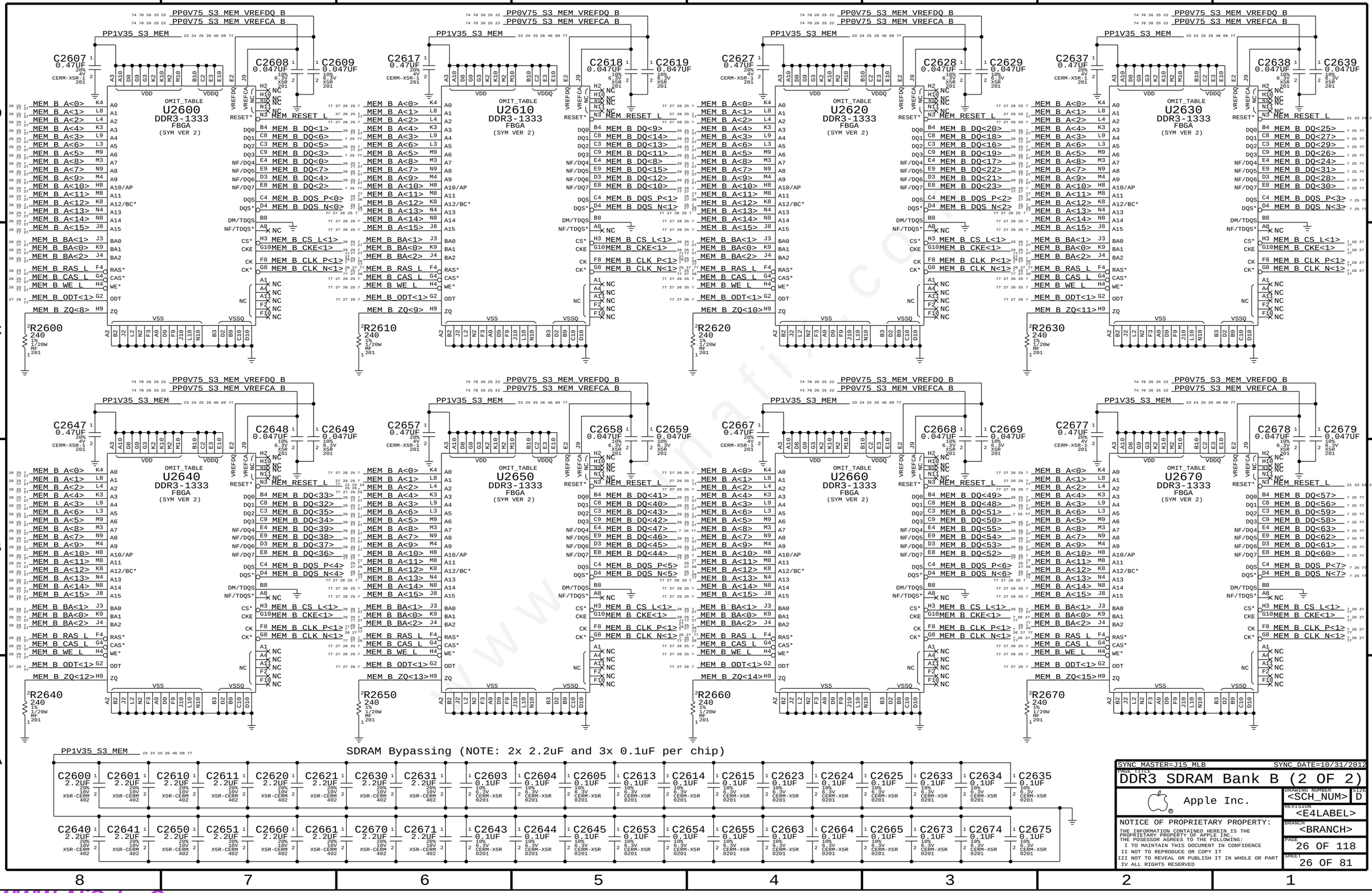

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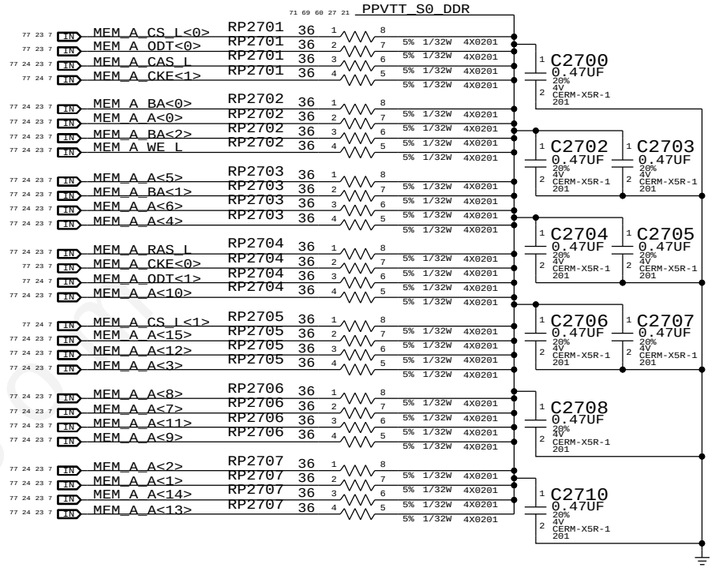
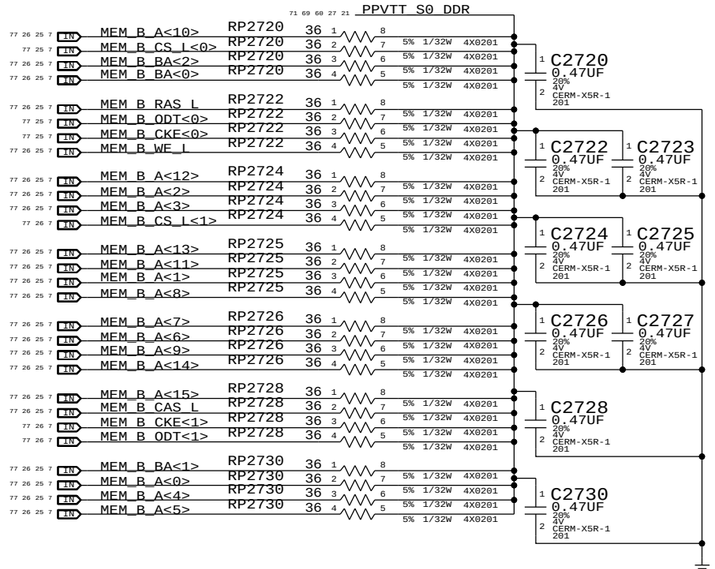
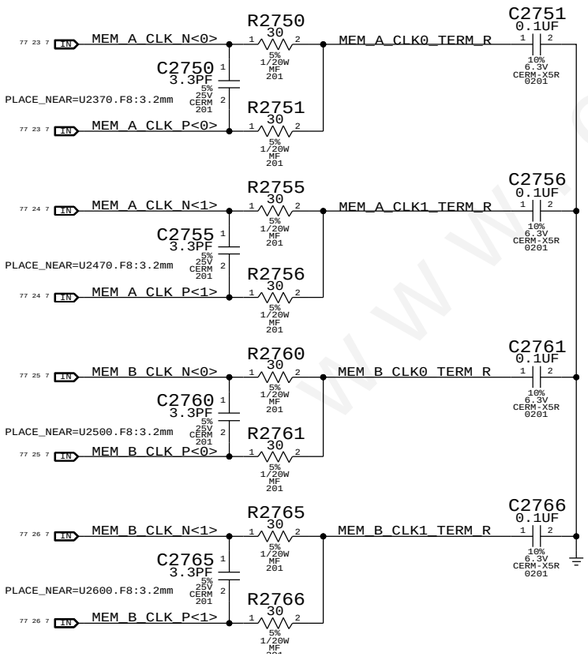
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: DDR3 Termination

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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CRITICAL
OMIT_TABLE

U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)

PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9 PERP_0
PCIE_TBT_R2D_C_N<0>	C2801 0.1UF	PCIE_TBT_R2D_N<0>	AA10 PERN_0
PCIE_TBT_R2D_C_P<1>	C2802 0.1UF	PCIE_TBT_R2D_P<1>	AA12 PERP_1
PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13 PERN_1
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15 PERP_2
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16 PERN_2
PCIE_TBT_R2D_C_P<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18 PERP_3
PCIE_TBT_R2D_C_N<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19 PERN_3

PETP_0	AD5	PCIE_TBT_D2R_C_P<0> → C2840 0.1UF → PCIE_TBT_D2R_P<0> OUT
PETN_0	AD7	PCIE_TBT_D2R_C_N<0> → C2841 0.1UF → PCIE_TBT_D2R_N<0> OUT
PETP_1	AD9	PCIE_TBT_D2R_C_P<1> → C2842 0.1UF → PCIE_TBT_D2R_P<1> OUT
PETN_1	AD11	PCIE_TBT_D2R_C_N<1> → C2843 0.1UF → PCIE_TBT_D2R_N<1> OUT
PETP_2	AD13	PCIE_TBT_D2R_C_P<2> → C2844 0.1UF → PCIE_TBT_D2R_P<2> OUT
PETN_2	AD15	PCIE_TBT_D2R_C_N<2> → C2845 0.1UF → PCIE_TBT_D2R_N<2> OUT
PETP_3	AD17	PCIE_TBT_D2R_C_P<3> → C2846 0.1UF → PCIE_TBT_D2R_P<3> OUT
PETN_3	AD19	PCIE_TBT_D2R_C_N<3> → C2847 0.1UF → PCIE_TBT_D2R_N<3> OUT

MISC

		TBT_PCIE_RESET_L IN → P5 PERST_OD_N
		TBT_PWR_ON_POC_RST_L IN → R4 PWR_ON_POC_RSTN
		TP_TBT_MONDC0 → AD23 MONDC0
		TP_TBT_MONDC1 → AC24 MONDC1
		DEBUG: For monitoring current/voltage
		TBT_MONOBSP → W18 MONOBSP
		TBT_MONOBSN → W16 MONOBSN
		DEBUG: For monitoring clock
		TBT_THERMD_P → AB7 THERMDA (Use AA8 GND ball for THERM_DN)
		TBT_SPI_MOSI → AA2 EE_DI
		TBT_SPI_MISO → Y3 EE_DO
		TBT_SPI_CS_L → T5 EE_CS_N
		TBT_SPI_CLK → U8 EE_CLK
		JTAG_TBT_TDI IN → W2 TDI
		JTAG_TBT_TMS IN → AB1 TMS
		JTAG_TBT_TCK IN → AA6 TCK
		JTAG_TBT_TDO OUT → U6 TDO
		TBT_TEST_EN → R6 TEST_EN
		TBT_TEST_PWR_GOOD → W8 TEST_PWR_GOOD
		RSENSE U20 TBT_RSENSE
		RBIAS W20 TBT_RBIAS → R2855 1K 1% 1/20W MF 201
		RSVD AD1, L8
		Used for straps in host mode
PCIE_RST_0_N	W6	TP_TBT_PCIE_RESET0_L
PCIE_RST_1_N	AB3	TBT_DFT_STRAP_1
PCIE_RST_2_N	AD3	TBT_ROM_SECURITY_XOR
PCIE_RST_3_N	V1	TBT_DFT_STRAP_3
PCIE_CLKREQ_OD_N	V3	TBT_CLKREQ_L OUT 11
REFCLK_100_IN_P	AB21	PCIE_CLK100M_TBT_P IN 11 76
REFCLK_100_IN_N	AD21	PCIE_CLK100M_TBT_N IN 11 76
XTAL_25_IN	AA24 75	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	AB23	NC_TBT_XTAL25OUT 72
TMU_CLK_OUT	AA4	TBT_TMU_CLK_OUT

DISPLAY PORT

DP_TBTSNK0_ML_P<3>	E14	DPSNK0_3_P
DP_TBTSNK0_ML_N<3>	D13	DPSNK0_3_N
DP_TBTSNK0_ML_P<2>	E16	DPSNK0_2_P
DP_TBTSNK0_ML_N<2>	D15	DPSNK0_2_N
DP_TBTSNK0_ML_P<1>	E18	DPSNK0_1_P
DP_TBTSNK0_ML_N<1>	D17	DPSNK0_1_N
DP_TBTSNK0_ML_P<0>	E20	DPSNK0_0_P
DP_TBTSNK0_ML_N<0>	D19	DPSNK0_0_N
DP_TBTSNK0_AUXCH_P	G4	DPSNK0_AUX_P
DP_TBTSNK0_AUXCH_N	G2	DPSNK0_AUX_N
DP_TBTSNK0_HPD	AB5	DPSNK0_HPD
DP_TBTSNK1_ML_P<3>	E6	DPSNK1_3_P
DP_TBTSNK1_ML_N<3>	D5	DPSNK1_3_N
DP_TBTSNK1_ML_P<2>	E8	DPSNK1_2_P
DP_TBTSNK1_ML_N<2>	D7	DPSNK1_2_N
DP_TBTSNK1_ML_P<1>	E10	DPSNK1_1_P
DP_TBTSNK1_ML_N<1>	D9	DPSNK1_1_N
DP_TBTSNK1_ML_P<0>	E12	DPSNK1_0_P
DP_TBTSNK1_ML_N<0>	D11	DPSNK1_0_N
DP_TBTSNK1_AUXCH_P	H3	DPSNK1_AUX_P
DP_TBTSNK1_AUXCH_N	H1	DPSNK1_AUX_N
DP_TBTSNK1_HPD	U4	DPSNK1_HPD

DPSRC_3_P	A14	NC_DP_TBTSRC_ML_CP<3>
DPSRC_3_N	B15	NC_DP_TBTSRC_ML_CN<3>
DPSRC_2_P	A12	NC_DP_TBTSRC_ML_CP<2>
DPSRC_2_N	B13	NC_DP_TBTSRC_ML_CN<2>
DPSRC_1_P	A10	NC_DP_TBTSRC_ML_CP<1>
DPSRC_1_N	B11	NC_DP_TBTSRC_ML_CN<1>
DPSRC_0_P	A8	NC_DP_TBTSRC_ML_CP<0>
DPSRC_0_N	B9	NC_DP_TBTSRC_ML_CN<0>
DPSRC_AUX_P	J4	NC_DP_TBTSRC_AUXCH_CP
DPSRC_AUX_N	J2	NC_DP_TBTSRC_AUXCH_CN
DPSRC_HPD_OD	AC2	DP_TBTSRC_HPD

		TBT_A_R2D_C_P<0> → G24 PA_CIO0_TX_P/DPSRC_0_P
		TBT_A_R2D_C_N<0> → E24 PA_CIO0_TX_N/DPSRC_0_N
		TBT_A_D2R_P<0> IN → G22 PA_CIO0_RX_P
		TBT_A_D2R_N<0> IN → E22 PA_CIO0_RX_N
		TBT_A_CONFIG1_BUF OUT → P1 PA_CONFIG1/CIO_0_LSEO
		TBT_A_CONFIG2_RC IN → K5 PA_CONFIG2/CIO_0_LSOE
		TBT_A_R2D_C_P<1> → L24 PA_CIO1_TX_P/DPSRC_2_P
		TBT_A_R2D_C_N<1> → J24 PA_CIO1_TX_N/DPSRC_2_N
		TBT_A_D2R_P<1> IN → L22 PA_CIO1_RX_P
		TBT_A_D2R_N<1> IN → J22 PA_CIO1_RX_N
		TBT_A_LSTX OUT → N8 PA_LSTX/CIO_1_LSEO
		TBT_A_LSRX IN → J6 PA_LSRX/CIO_1_LSOE
		DP_TBTPA_ML_C_P<1> OUT → A16 PA_DPSRC_1_P
		DP_TBTPA_ML_C_N<1> OUT → B17 PA_DPSRC_1_N
		DP_TBTPA_ML_C_P<3> OUT → A18 PA_DPSRC_3_P
		DP_TBTPA_ML_C_N<3> OUT → B19 PA_DPSRC_3_N
		DP_TBTPA_AUXCH_C_P BI → L4 PA_AUX_P
		DP_TBTPA_AUXCH_C_N BI → L2 PA_AUX_N
		DP_TBTPA_HPD IN → M3 PA_DPSRC_HPD
		TBT_A_HV_EN → R8 GPIO_0/PA_HV_EN/BYP0
		TBT_A_CIO_SEL → N2 GPIO_10/PA_CIO_SEL/BYP1
		TBT_A_DP_PWRDN → P3 GPIO_12/PA_DP_PWRDN/BYP2

		GPIO_2/TMU_CLK_IN/AC_PRESENT U2 TBT_GPIO2
		GPIO_3/FORCE_PWR L6 TBT_PWR_EN IN 20
		GPIO_4/WAKE_OD_N H5 SMC_PME_S4_DARK_L OUT 20 41 42 43
		GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD Y7 TBT_CIO_PLUG_EVENT_L OUT 14 20
		GPIO_6_OD/CIO_SDA_OD Y1 HDMITBTMUX_SEL_TBT IN 28 70
		GPIO_7_OD/CIO_SCL_OD T7 TBT_GPIO7
		GPIO_8/EN_CIO_PWR_OD* V7 TBT_EN_CIO_PWR_L OUT 28 29
		GPIO_9/SX_CTRL_OD* M7 TBT_BATLOW_L IN 28 30
		GPIO_14 T1 TBTDP_AUXIO_EN OUT 28 31 32
		GPIO_15 T3 TBT_DDC_XBAR_EN_L OUT 28 33
		TBT_B_R2D_C_P<0> → R24 PB_CIO2_TX_P/DPSRC_0_P
		TBT_B_R2D_C_N<0> → N24 PB_CIO2_TX_N/DPSRC_0_N
		TBT_B_D2R_P<0> IN → R22 PB_CIO2_RX_P
		TBT_B_D2R_N<0> IN → N22 PB_CIO2_RX_N
		TBT_B_CONFIG1_BUF OUT → D3 PB_CONFIG1/CIO_2_LSEO
		TBT_B_CONFIG2_RC IN → M1 PB_CONFIG2/CIO_2_LSOE
		TBT_B_R2D_C_P<1> → W24 PB_CIO3_TX_P/DPSRC_2_P
		TBT_B_R2D_C_N<1> → U24 PB_CIO3_TX_N/DPSRC_2_N
		TBT_B_D2R_P<1> IN → W22 PB_CIO3_RX_P
		TBT_B_D2R_N<1> IN → U22 PB_CIO3_RX_N
		TBT_B_LSTX OUT → M5 PB_LSTX/CIO_3_LSEO
		TBT_B_LSRX IN → P7 PB_LSRX/CIO_3_LSOE
		DP_TBTPB_ML_C_P<1> OUT → A20 PB_DPSRC_1_P
		DP_TBTPB_ML_C_N<1> OUT → B21 PB_DPSRC_1_N
		DP_TBTPB_ML_C_P<3> OUT → A22 PB_DPSRC_3_P
		DP_TBTPB_ML_C_N<3> OUT → B23 PB_DPSRC_3_N
		DP_TBTPB_AUXCH_C_P BI → K3 PB_AUX_P
		DP_TBTPB_AUXCH_C_N BI → K1 PB_AUX_N
		DP_TBTPB_HPD IN → N6 PB_DPSRC_HPD
		TBT_B_HV_EN → F1 GPIO_1/PB_HV_EN/BYP0
		TBT_B_CIO_SEL → R2 GPIO_11/PB_CIO_SEL/BYP1
		TBT_B_DP_PWRDN → F3 GPIO_13/PB_DP_PWRDN/BYP2

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

PP3V3_TBTLC

R2890 3.3K 5% 1/20W MF 201
R2891 3.3K 5% 1/20W MF 201
C2890 1UF 10% 6.3V CERM 402 (BYPASS=U2890:2mm)
R2892 3.3K 5% 1/20W MF 201
R2893 3.3K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U2890 4MBIT W25X40CLXIG USON

(TBT_SPI_MOSI)	5	DI/IO0
(TBT_SPI_CLK)	6	CLK
(TBT_SPI_CS_L)	1	CS*
TBTROM_WP_L	3	WP*
TBTROM_HOLD_L	7	HOLD*
	2	DO/IO1 (TBT_SPI_MISO)
	8	VCC
	4, 9	GND THRM_PAD

OMIT
R2815 NOSTUFF 0201

R2829 10K 5% 1/20W MF 201
R2825 100 5% 1/20W MF 201

R2831 100K 5% 1/20W MF 201
R2830 100K 5% 1/20W MF 201

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.

If strap != bit then security is enabled?

NO STUFF R2867 10K 5% 1/20W MF 201

R2861 10K 5% 1/20W MF 201
R2862 10K 5% 1/20W MF 201
R2863 10K 5% 1/20W MF 201

Divides 3.3V to 1.8V
R2895 806 1% 1/20W MF 201
SYSCLK_CLK25M_TBT IN 19 75

PP3V3_TBTLC 69 29 28 20 19
PP3V3_S4_TBT 69 46 30 29 28

NO STUFF R2899 10K 5% 1/20W MF 201
R2896 1K 5% 1/20W MF 201

R2881 100K 5% 1/20W MF 201
R2880 100K 5% 1/20W MF 201
R2882 100K 5% 1/20W MF 201

TBT_EN_CIO_PWR_L 29 28
TBT_DDC_XBAR_EN_L 33 28
HDMITBTMUX_SEL_TBT 70 28
TBTDP_AUXIO_EN 32 31 28
DP_TBTSRC_HPD 28

PP3V3_TBTLC 19 20 28 29 69

R2878 100K 5% 1/20W MF 201
R2879 100K 5% 1/20W MF 201

R2832 100K 5% 1/20W MF 201
R2883 100K 5% 1/20W MF 201

PP3V3_S4_TBT 69 46 30 29 28

R2884 100K 5% 1/20W MF 201
NO STUFF R2885 10K 5% 1/20W MF 201
NO STUFF R2886 10K 5% 1/20W MF 201

TBT_BATLOW_L 30 28
TBT_A_DP_PWRDN 31 28
TBT_B_DP_PWRDN 32 28
TBT_A_HV_EN 31 30 28
TBT_B_HV_EN 33 32 28

R2888 10K 5% 1/20W MF 201
R2887 10K 5% 1/20W MF 201

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF	DP_TBTSNK1_AUXCH_N

All: 10% 16V X5R-CERM 0201

SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

PAGE TITLE: Thunderbolt Host (1 of 2)

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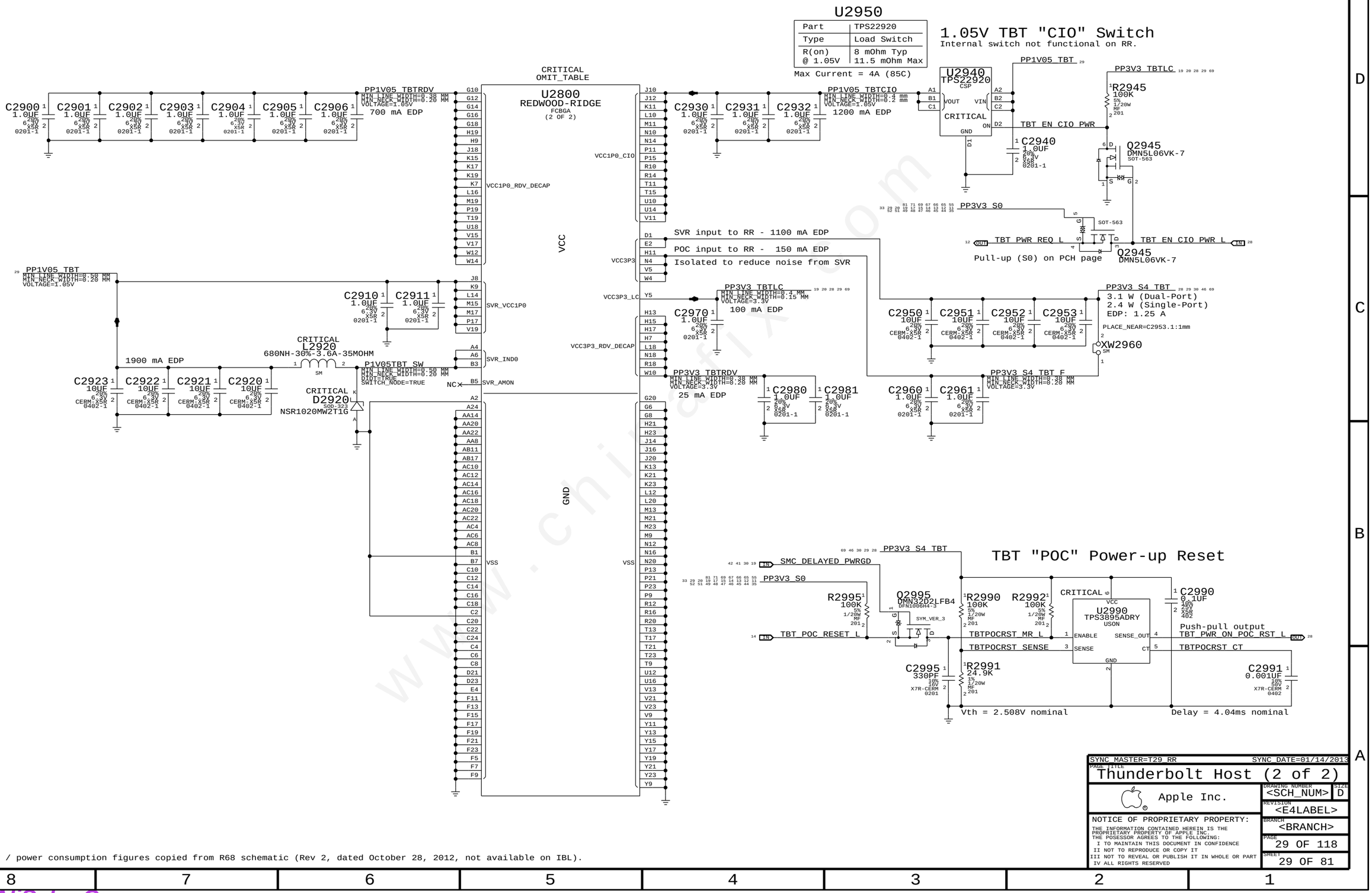

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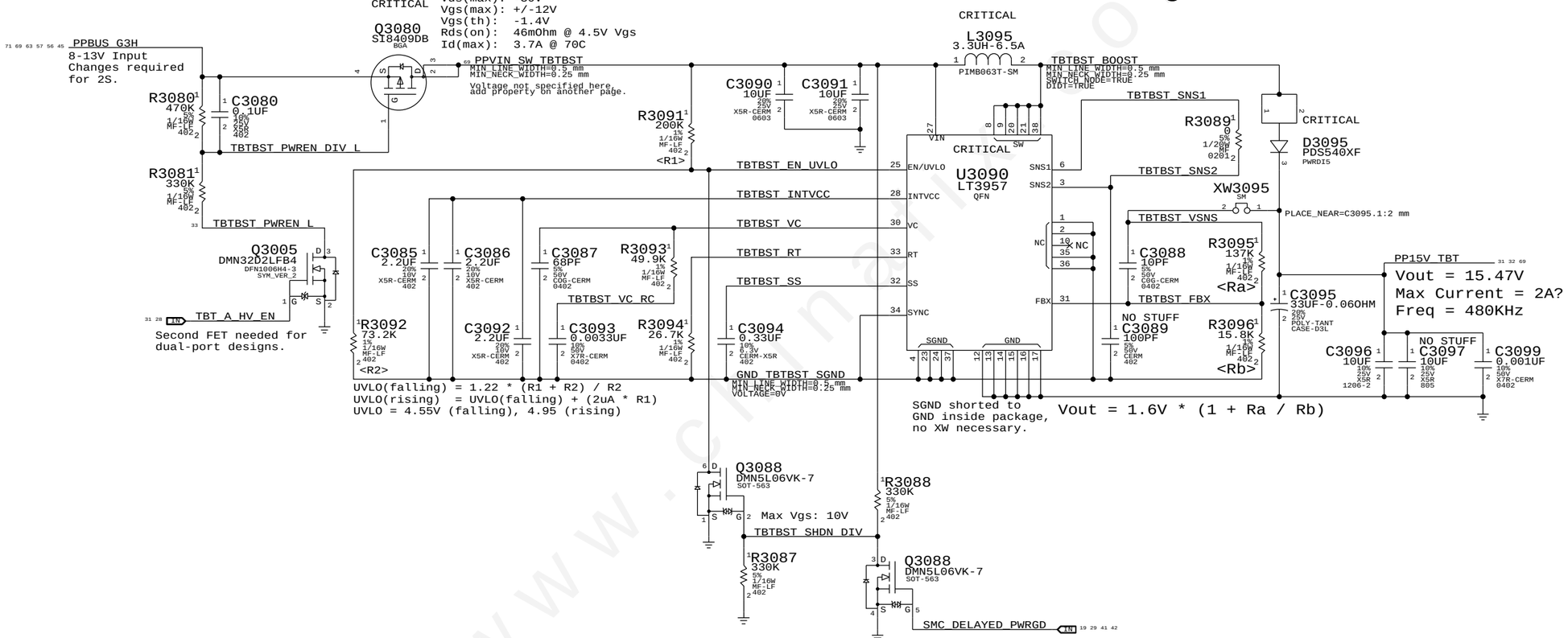
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

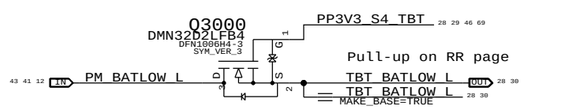
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



BATLOW# Isolation



SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

PAGE TITLE
Thunderbolt Mobile Support

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

PP3V3_S5

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 603
C3281 0.1UF 10% 16V X5R-CERM 0201
PP15V_TBT 15.75V Max
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 16V X5R 402
CRITICAL U3210 CD3211A0RGPR QFN
V3P3 V3P3OUT VHV OUT ENHVU FAULTZ EN ISET_V3P3 HV_EN ISET_S0 S0 ISET_S3 GND THRM PAD
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V 402
PP3V3_S4_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)
PP3V3RHV_S4_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_R_L
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V R3210 22.6K 1% 1/20W MF 201
TBTHV:P15V R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>
12V: See below
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
TBTHV:P15V R3213 22.6K 1% 1/20W MF 201 <RHVS3>
TBTHV:P15V R3214 22.6K 1% 1/20W MF 201 <RHVS0> ILIM = 40000 / RISET
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3220 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V_201 CERM-X5R-1
C3276 0.47UF 20% 4V_201 CERM-X5R-1
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201

TBT_A_D2R_N<1> → TBT_A_D2R_C_N<1>
TBT_A_D2R_P<1> → TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N → DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_C_P → DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF → TBT_A_CONFIG1_RC
DP_TBTPA_ML_C_P<1> → DP_TBTPA_ML_P<1>
DP_TBTPA_ML_C_N<1> → DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD

TB- TB+ AUX- AUX+ DDC_DAT DDC_CLK CA_DETOUT DP+ DP- LSTX (IPU) LSRX (IPD) HPDOUT
TB_ENA AUXIO_EN DP_PD (IPU)AUXIO- (IPD)AUXIO+ CA_DET DPML0+ DPML0- HPD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
GND_THMPAD

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V)
R3201 12 5% 1/20W MF 201

TBT Dir DP Dir

TBT_A_D2R_P<0> → TBT_A_D2R_C_P<0>
TBT_A_D2R_N<0> → TBT_A_D2R_C_N<0>
GND_VOID=TRUE (Both C's)
C3274 0.47UF 20% 4V_201 CERM-X5R-1
C3275 0.47UF 20% 4V_201 CERM-X5R-1
R3294 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3295 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
TBT: RX_0

DP_TBTPA_ML_C_P<3> → DP_TBTPA_ML_P<3>
DP_TBTPA_ML_C_N<3> → DP_TBTPA_ML_N<3>
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
TBT: Unused

TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT: RX_1

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL
SHIELD PINS
J3200 MDP-J44 F-RT-TH
PORT B
SHIELD PINS
514-0876

HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN GND0

TBTACONN_1_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V) (0-18.9V)
C3205 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V) (0-18.9V)
C3206 0.01UF 10% 25V X5R-CERM 0201

DP Dir TBT Dir
TBT_A_R2D_P<0> → TBT_A_R2D_C_P<0>
TBT_A_R2D_N<0> → TBT_A_R2D_C_N<0>
TBT: TX_0
TBT: LSX_R2P/P2R (P/N)
TBT_A_R2D_P<1> → TBT_A_R2D_C_P<1>
TBT_A_R2D_N<1> → TBT_A_R2D_C_N<1>
TBT: TX_1

GND_VOID=TRUE (Both C's)
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT
15.75V Max
CRITICAL C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3380 22UF 20% 6.3V X5R-CERM 603
C3381 0.1UF 10% 16V X5R-CERM 0201
C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 16V X5R 402
CRITICAL U3310 CD3211A0RGPR QFN
C3385 0.1UF 10% 16V X5R-CERM 0201
C3386 10UF 20% 6.3V CERM-X5R 0402
C3311 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTBPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)
PP3V3RHV_S4_TBTBPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
S4_PWR_EN
TBT_B_HV_EN
PM_SLP_S3_R_L
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTHV:P15V R3310 22.6K 1% 1/20W MF 201
TBTHV:P15V R3311 22.6K 1% 1/20W MF 201
R3312 36.5K 1% 1/20W MF 201 <RV3P3>
12V: See below
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V R3313 22.6K 1% 1/20W MF 201 <RHVS3>
TBTHV:P15V R3314 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

CRITICAL L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
C3300 0.01UF 10% 50V X7R-CERM 0402
R3301 12 5% 1/20W MF 201
C3301 0.01UF 10% 50V X7R-CERM 0402
TBTBCONN_20_RC (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V)
TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1
C3302 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

GND_VOID=TRUE (Both C's)
TBT_B_D2R_P<0> TBT_B_D2R_N<0> C3374 0.47UF 20% 4V 201 CERM-X5R-1 C3375 0.47UF 20% 4V 201 CERM-X5R-1
TBT_B_D2R_C_P<0> TBT_B_D2R_C_N<0>
R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
DP_TBTPB_ML_C_P<3> DP_TBTPB_ML_C_N<3> C3378 0.22UF 20% 6.3V X5R 0201 C3379 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_P<3> DP_TBTPB_ML_N<3>
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201
TBT_B_D2R1_AUXDDC_P TBT_B_D2R1_AUXDDC_N
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201

CRITICAL J3200 MDP-J44 F-RT-TH 514-0876
SHIELD PINS S5 S4 S3 S2 S1
PORT A SHIELD PINS S23 S11 S10 S9 S8 S7 S6
A2 HPD
A4 CONFIG1
A6 CONFIG2
A8 GND2
A10 ML_LANE3P
A12 ML_LANE3N
A14 GND4
A16 AUX_CHP
A18 AUX_CHN
A20 DP_PWR
GND0 A1
ML_LANE0P A3
ML_LANE0N A5
GND1 A7
ML_LANE1P A9
ML_LANE1N A11
GND3 A13
ML_LANE2P A15
ML_LANE2N A17
RETURN A19

TBTBCONN_1_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V) (0-18.9V)
GND_VOID=TRUE C3305 0.01UF 10% 25V X5R-CERM 0201
DP Dir TBT Dir
TBT_B_R2D_P<0> TBT_B_R2D_N<0>
TBT: TX_0
TBTBCONN_7_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V) (0-18.9V)
GND_VOID=TRUE C3306 0.01UF 10% 25V X5R-CERM 0201
TBT_B_R2D_P<1> TBT_B_R2D_N<1>
TBT: TX_1
DP_B_LSX_ML_P<1> DP_B_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

GND_VOID=TRUE (Both C's)
C3370 0.22UF 20% 6.3V X5R 0201 C3371 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<0> TBT_B_R2D_C_N<0>
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
C3372 0.22UF 20% 6.3V X5R 0201 C3373 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<1> TBT_B_R2D_C_N<1>
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201
470K R's for ESD protection on AC-coupled signals.

PP3V3_S4_TBTBPWR
C3320 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3320 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
TB- TB+ AUX- AUX+ DDC_DAT DDC_CLK CA_DETOUT DP+ DP- LSTX (IPU) LSRX (IPD) HPDOUT
TB_ENA AUXIO_EN DP_PD (IPU)AUXIO- (IPD)AUXIO+ CA_DET DPML0+ DPML0- HPD GND THMPAD
TBT_B_CIO_SEL TBTDP_AUXIO_EN TBT_B_DP_PWRDN TBT_B_D2R1_AUXDDC_N TBT_B_D2R1_AUXDDC_P
TBT: RX_1
TBT_B_CONFIG1_RC
TBT_B_HPD
DP_B_LSX_ML_P<0> DP_B_LSX_ML_N<0>
TBT: LSX_A_R2P/P2R (P/N)
DP_TBTPB_AUXCH_C_N DP_TBTPB_AUXCH_C_P C3330 0.1UF 10% 16V X5R-CERM 0201 C3331 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPB_AUXCH_N DP_TBTPB_AUXCH_P
DP_TBTPB_DDC_DATA DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1> DP_TBTPB_ML_C_N<1> C3332 0.22UF 20% 6.3V X5R 0201 C3333 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_P<1> DP_TBTPB_ML_N<1>
TBT_B_LSTX TBT_B_LSRX
DP_TBTPB_HPD

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012
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Apple Inc.
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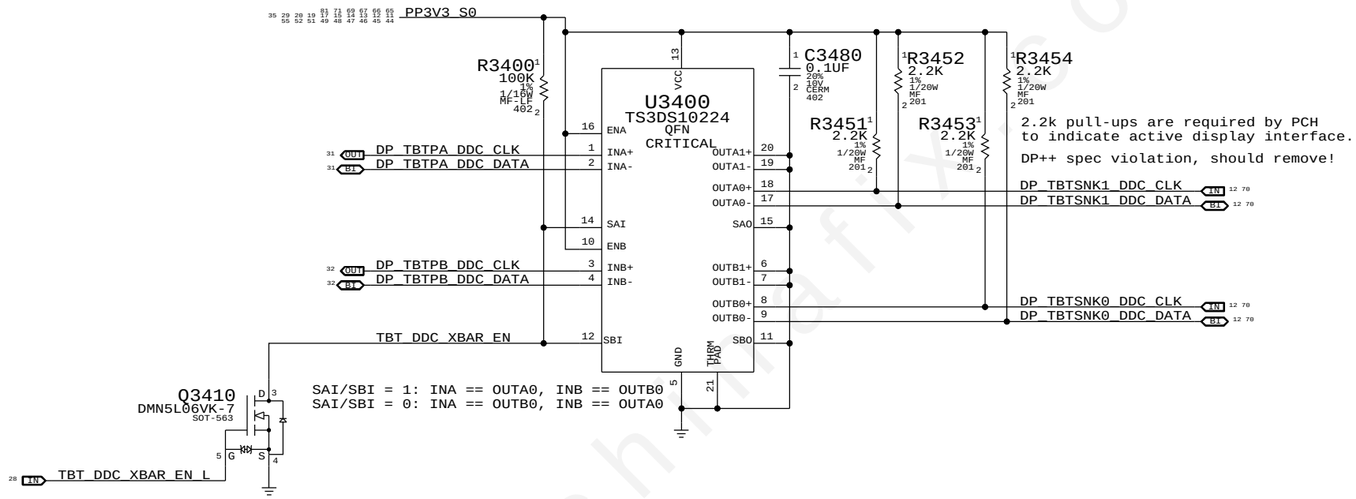
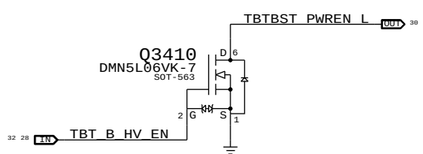
DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



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PAGE TITLE	DDC Crossbar
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

AIRPORT

BLUETOOTH

Supervisor & CLKREQ # Isolation

Delay = 130 ms +/- 20%

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

X29C CONNECTOR

Apple Inc.

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OOB Isolation

PP3V3_S0SW_SSD

BYPASS=U3710:5 mm
C3718 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3710 08
SMC_OOB1_R2D_L (IN)
NC

PP3V3_S0

BYPASS=U3711:5 mm
C3719 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3711 08
SMC_OOB1_D2R_L (OUT)
NC

PLACE_NEAR=J3700.1:3mm
CRITICAL
L3700 FERR-26-OHM-6A 0603

PP3V3_S0SW_SSD
PP3V3_S0SW_SSD_FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.15mm
VOLTAGE=3.3V

C3701 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=L3700.1:1mm

C3702 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=L3700.1:1mm

514S0449
CRITICAL
J3700 SSD-GS3 F-RT-SM

R3700 100K 1% 1/20W MF 0201

GND_VOID	1	53	GND_VOID		
	2	52	SMC_OOB1_R2D_CONN_L		
	3	51	SMC_OOB1_D2R_CONN_L		
	4				
	5	50	SSD_PCIE_SEL_L	OUT	18
PP3V3_S0	6	49	SSD_DEVSLP	IN	20
SSD_RESET_CONN_L	7	48	SMC_PWRFAIL_WARN_L	IN	41
NC_SSD_MFG_RSVD	8	47	SSD_PWR_FET_EN	IN	35 65
	9				
	10	46			
PCIE_SSD_R2D_C_N<3>	11	45	PCIE_SSD_D2R_N<3>	OUT	13 76
PCIE_SSD_R2D_C_P<3>	12	44	PCIE_SSD_D2R_P<3>	OUT	13 76
	13	43			
PCIE_SSD_R2D_C_N<2>	14	42	PCIE_SSD_D2R_N<2>	OUT	13 76
PCIE_SSD_R2D_C_P<2>	15	41	PCIE_SSD_D2R_P<2>	OUT	13 76
	16	40			
	17	39			
PCIE_SSD_R2D_C_N<1>	18	38	PCIE_SSD_D2R_N<1>	OUT	13 76
PCIE_SSD_R2D_C_P<1>	19	37	PCIE_SSD_D2R_P<1>	OUT	13 76
	20	36			
PCIE_SSD_R2D_C_N<0>	21	35	PCIE_SSD_D2R_N<0>	OUT	13 76
PCIE_SSD_R2D_C_P<0>	22	34	PCIE_SSD_D2R_P<0>	OUT	13 76
	23	33			
SSD_CLKREQ_CONN_L	24				
	25	32			
	26	31	PCIE_CLK100M_SSD_N	IN	11 76
	27	30	PCIE_CLK100M_SSD_P	IN	11 76
	28	29			
	54	59			
	55	60			
	56	61			
	57	62			
	58	63			

Gumstick3 Connector

PCIE_SSD_R2D_C_N<3> C3710 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
PCIE_SSD_R2D_C_P<3> C3711 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
PCIE_SSD_R2D_C_N<2> C3712 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
PCIE_SSD_R2D_C_P<2> C3713 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
PCIE_SSD_R2D_C_N<1> C3714 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
PCIE_SSD_R2D_C_P<1> C3715 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
PCIE_SSD_R2D_C_N<0> C3716 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
PCIE_SSD_R2D_C_P<0> C3717 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

Supervisor & CLKREQ# Isolation

Delay = ~55ms

PP3V3_S0SW_SSD
PP3V42_G3H

R3740 100K 5% 1/20W MF 201
R3741 232K 1% 1/20W MF 201
R3742 100K 1% 1/20W MF 201

CRITICAL
U3740 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, IN, OUT (OD), THRM PAD, GND

C3740 0.1UF 10% 6.3V CERM-X5R 0201

P3V3SSD_VMON
SSD_RESET_L (IN 20)
SSD_PWR_FET_EN (IN 35 65)
SSD_CLKREQ_L (OUT 11)

APN 343S0511

SSD_PWR_FET_EN = SSD_PWR_FET_EN
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_MLB_KEPLER SYNC_DATE=06/08/2013

PAGE TITLE: SSD Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE

U3900
BCM15700
FBGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE

U3900
BCM15700
FBGA
SYM 2 OF 3
CRITICAL
OMIT_TABLE

L3902 1.0UH-1.6A-55MOHM
L3901 1.0UH-1.6A-55MOHM
L3903 220-OHM-1.4A
L3904 220-OHM-1.4A
L3906 22NH

PP1V35_CAM
PP1V35_DDR_CLK
PP1V35_CAM_SRVLXD_PHASE
PP1V8_CAM
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PVDD_FLT
PP1V2_CAM_XTALPCIEVDD
PP1V2_CAM_SRVLXC_PHASE
PP3V3_S3RS0_CAMERA
(=PP3V3_S3RS0_CAMERA)
GND_CAM_PVSSD
GND_CAM_PVSSC
XW3900
XW3901
PU on PCH page
A1 SILICON BUG
PU = 1.35V
PU = 25MHz
BYPASS=U3900.K13:2.54MM
PLACE_NEAR=U3900.K13:4MM
PLACE_NEAR=U3900.M13:4MM
PLACE_NEAR=U3900.M14:2.54MM
BYPASS=U3900.F15:2.54MM
BYPASS=U3900.G15:2.54MM
BYPASS=U3900.D7:2.54MM
BYPASS=U3900.J1:2.54MM
BYPASS=U3900.L7:2.54MM
BYPASS=U3900.D6:2.54MM
BYPASS=U3900.B6:2.54MM
BYPASS=U3900.F6:2.54MM
BYPASS=U3900.F9:2.54MM
BYPASS=U3900.L9:2.54MM
BYPASS=U3900.5MM
BYPASS=U3900.3MM

SYNC_MASTER=CLEAN_MLB_KEPLER
SYNC_DATE=06/13/2013
PAGE TITLE: Camera 1 of 2
Apple Inc.
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PP1V35_CAM

PP0V675_CAM_VREF

R4000 0 0201 5% 1/20W MF

PP0V675_MEM_CAM_VREFDQ
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.675V

PP0V675_MEM_CAM_VREFCA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.675V

R4022 1K 1% 1/20W MF 201

R4023 1K 1% 1/20W MF 201

R4002 1K 5% 1/20W MF 201

NOSTUFF
R4003 1K 5% 1/20W MF 201

BYPASS=U4000.A1:4mm
C4002 10UF 20% 6.3V X5R 402

BYPASS=U4000.B2:4mm
C4003 10UF 20% 6.3V X5R 402

C4004 0.47UF 20% 6.3V CERM-X5R-1 201

C4005 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U4000.D2:4mm
C4006 2.2UF 20% 6.3V X5R-CERM 402

C4007 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U4000.K2:4mm
C4008 2.2UF 20% 6.3V X5R-CERM 402

C4009 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U4000.H9:4mm

BYPASS=U4000.R9:4mm

C4010 0.1UF 10% 6.3V CERM-X5R 0201

C4011 0.1UF 10% 6.3V CERM-X5R 0201

U4000
4GB-DDR3-256MX16
FBGA
K4B4G1646B-HYK0

CRITICAL

OMIT_TABLE

VDDQ: A1 A8 C1 C9 D2 E9 F1 H2 H9

VDD: B2 D9 G7 K2 K8 M1 N9 R1 R9

M8 VREFCA

H1 VREFDQ

J1 NC
J9 NC
L1 NC
L9 NC
M7 NC

MEM_CAM_A<0>	N3	A0	
MEM_CAM_A<1>	P7	A1	
MEM_CAM_A<2>	P3	A2	
MEM_CAM_A<3>	N2	A3	
MEM_CAM_A<4>	P8	A4	
MEM_CAM_A<5>	P2	A5	
MEM_CAM_A<6>	R8	A6	
MEM_CAM_A<7>	R2	A7	
MEM_CAM_A<8>	T8	A8	
MEM_CAM_A<9>	R3	A9	
MEM_CAM_A<10>	L7	A10/AP	
MEM_CAM_A<11>	R7	A11	
MEM_CAM_A<12>	N7	A12/BC*	
MEM_CAM_A<13>	T3	A13	
MEM_CAM_A<14>	T7	A14	
MEM_CAM_BA<0>	M2	BA0	
MEM_CAM_BA<1>	N8	BA1	
MEM_CAM_BA<2>	M3	BA2	
MEM_CAM_RAS_L	J3	RAS*	
MEM_CAM_CAS_L	K3	CAS*	
MEM_CAM_WE_L	L3	WE*	
MEM_CAM_CLK_P	J7	CK	
MEM_CAM_CLK_N	K7	CK*	
MEM_CAM_CKE	K9	CKE	
MEM_CAM_CS_L	L2	CS*	
MEM_CAM_ODT	K1	ODT	
MEM_CAM_ZQ_DDR	L8	ZQ	
MEM_CAM_RESET_L	T2	RESET*	

DQL0	E3	MEM_CAM_DQ<0>	B1
DQL1	F7	MEM_CAM_DQ<1>	B1
DQL2	F2	MEM_CAM_DQ<2>	B1
DQL3	F8	MEM_CAM_DQ<3>	B1
DQL4	H3	MEM_CAM_DQ<4>	B1
DQL5	H8	MEM_CAM_DQ<5>	B1
DQL6	G2	MEM_CAM_DQ<6>	B1
DQL7	H7	MEM_CAM_DQ<7>	B1
DQSL	F3	MEM_CAM_DQS_P<0>	B1
DQSL*	G3	MEM_CAM_DQS_N<0>	B1
DQSU	C7	MEM_CAM_DQS_P<1>	B1
DQSU*	B7	MEM_CAM_DQS_N<1>	B1
DQU0	D7	MEM_CAM_DQ<8>	B1
DQU1	C3	MEM_CAM_DQ<9>	B1
DQU2	C8	MEM_CAM_DQ<10>	B1
DQU3	C2	MEM_CAM_DQ<11>	B1
DQU4	A7	MEM_CAM_DQ<12>	B1
DQU5	A2	MEM_CAM_DQ<13>	B1
DQU6	B8	MEM_CAM_DQ<14>	B1
DQU7	A3	MEM_CAM_DQ<15>	B1
DML	E7	MEM_CAM_DM<0>	IN
DMU	D3	MEM_CAM_DM<1>	IN

VSSQ: B1 B9 D1 D8 E2 E8 F9 G1 G9

VSS: A9 B3 E1 G8 J2 J8 M1 M9 P1 P9 T1 T9

R4020 84.5 1% 1/20W MF 201

NO STUFF
R4021 82 1% 1/20W MF 201

MEM_CAM_CKE_R

NO STUFF
R4006 100PF 5% 25V NP0-CERM 0201

R4004 240 1% 1/20W MF 201

PP1V8_CAM

R4005 100K 5% 1/20W MF 201

CAM_WAKE:YES
R4030 0 0201 5% 1/20W MF

CAM_SENSOR_WAKE_L_CONN → CAM_SENSOR_WAKE_L

CAM_WAKE:NO
R4031 0 5% 1/20W MF 0201

PCIE_CAMERA_R2D_C_P	C4033 0.1UF	PCIE_CAMERA_R2D_P	OUT
PCIE_CAMERA_R2D_C_N	C4032 0.1UF	PCIE_CAMERA_R2D_N	OUT
PCIE_CAMERA_D2R_C_P	C4031 0.1UF	PCIE_CAMERA_D2R_P	OUT
PCIE_CAMERA_D2R_C_N	C4030 0.1UF	PCIE_CAMERA_D2R_N	OUT
PCIE_CLK100M_CAMERA_P	C4061 0.1UF	PCIE_CLK100M_CAMERA_C_P	OUT
PCIE_CLK100M_CAMERA_N	C4062 0.1UF	PCIE_CLK100M_CAMERA_C_N	OUT

(all 10% 16V X5R-CERM 0201)

remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR

CRITICAL
J4002
CCR20-AK7100-1
F-RT-SM

1		
2	MIPI_CLK_CONN_N	79 71
3	MIPI_CLK_CONN_P	79 71
4	CAM_SENSOR_WAKE_L_CONN	37 71
5	MIPI_DATA_CONN_N	79 71
6	MIPI_DATA_CONN_P	79 71
7		
8	SMBUS_SMC_0_S0_SDA	IO 41 44 48 71 80
9	SMBUS_SMC_0_S0_SCL	IO 41 44 48 71 80
10	I2C_CAM_SCK	IN 36 71
11	I2C_CAM_SDA	IO 36 71
12	PP5V_S3RS0_ALSCAM_F	71
13		
14		

ALS

518S0892

L4009 90-OHM-50MA TCM0605-1
MIPI_CLK_N → MIPI_CLK_CONN_N
MIPI_CLK_P → MIPI_CLK_CONN_P
PLACE_NEAR=J4002.2:2.54MM
CRITICAL

L4007 90-OHM-50MA TCM0605-1
MIPI_DATA_N → MIPI_DATA_CONN_N
MIPI_DATA_P → MIPI_DATA_CONN_P
PLACE_NEAR=J4002.5:2.54MM
CRITICAL

L4010 FERR-120-OHM-1.5A 0402-LF
PP5V_S0 → 18 19 49 50 58 59 62 63 65 66 69 70 71

C4013 0.1UF 10% 16V CERM 402

NOSTUFF
L4011 FERR-120-OHM-1.5A 0402-LF
PP5V_S3 → 21 60 65 66 69 71

77.2 mA nominal max
96.2 mA peak

SYSCLK_CLK25M_CAMERA

C4015 12PF 5% 25V NP0-C0G-CERM 0201 CAM_XTAL:YES

C4014 12PF 5% 25V NP0-C0G-CERM 0201 CAM_XTAL:YES

CRITICAL
Y4000
NC NC
SM-3.2X2.5MM
25.000MHZ-12PF-20PPM
CAM_XTAL:YES

CAM_XTAL:YES
R4007 0 0201 5% 1/20W MF

CLK25M_CAM_XTALP → CLK25M_CAM_XTALP_R

NOSTUFF
R4012 1M 1% 1/20W MF 201

CLK25M_CAM_XTALN

R4008 0 0201 5% 1/20W MF
CLK25M_CAM_CLKP

R4009 0 5% 1/20W MF 0201
NO STUFF

R4010 0 5% 1/20W MF 0201
NO STUFF

CLK25M_CAM_CLKN → OUT

C4016 100PF 5% 25V NP0-CERM 0201

NOTE: TBD PPM crystal required

SYNC_MASTER=CLEAN_MLB_KEPLER
SYNC_DATE=06/13/2013

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USB Port Power Switch

71 69 68 67 66 65 61 51 PP5V_S4

71 68 66 41 34 21 12 PM_SLP_S4_L

R4690 0 5% 1/16W MF-LF 402

USB_PWR_EN

18 OUT USB_EXTA_OC_L

CRITICAL
U4600
TPS2557DRB
SON

IN_0 IN_1 FAULT* EN OUT1 OUT2 ILIM THRM GND PAD

USB_ILIM

R4601 22.1K 1% 1/20W MF 201

USB_ILIM_R

R4600 22.1K 1% 1/16W MF 402

NOSTUFF C4692 0.47UF 10% 10V X5R 0402

CRITICAL C4696 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

C4690 10UF 20% 6.3V X5R 603

C4691 0.1UF 10% 10V X5R CERM 402

C4695 10UF 20% 6.3V X5R 603

PP5V_S3_LTUSB_A_ILIM
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CRITICAL L4605 FERR-120-OHM-3A 0603

C4605 0.01UF 10% 16V X7R-CERM 0402

PP5V_S3_LTUSB_A_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin

CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

USB/SMC Debug Mux

50 44 43 42 41 39 35 19 71 69 68 67 66 PP3V42_G3H

C4650 0.1UF 20% 10V CERM 402

R4650 100K 5% 1/16W MF-LF 402

VCC

75 42 41 IN SMC_DEBUGPRT_RX_L

75 42 41 OUT SMC_DEBUGPRT_TX_L

U4650
PI3USB102EZLE
TQFN
CRITICAL

M+ M- D+ D- OE* SEL Y+ Y-

75 13 B1 USB_EXTA_P

75 13 B1 USB_EXTA_N

SEL 10

SMC_DEBUGPRT_EN_L IN 41

SEL=0 Choose SMC
SEL=1 Choose USB

GND

SIGNAL_MODEL=MOJO_MUX_USBONLY

NOSTUFF R4651 0 5% 1/20W MF 0201

NOSTUFF R4652 0 5% 1/20W MF 0201

75 USB_EXTA_MUXED_N

75 USB_EXTA_MUXED_P

CRITICAL L4600 90-OHM-50MA TCM0605-1

CRITICAL D4601 ESD0P2RF-02LS TSSLP-2-1

CRITICAL D4600 ESD0P2RF-02LS TSSLP-2-1

75 OUT USB3_EXTA_D2R_N

75 OUT USB3_EXTA_D2R_P

CRITICAL D4610 ESD0P2RF-02LS TSSLP-2-1

CRITICAL D4611 ESD0P2RF-02LS TSSLP-2-1

75 IN USB3_EXTA_R2D_C_N

C4610 0.1UF 10% 16V X5R-CERM 0201

GND_VOID=TRUE

75 IN USB3_EXTA_R2D_C_P

C4611 0.1UF 10% 16V X5R-CERM 0201

GND_VOID=TRUE

CRITICAL D4612 ESD0P2RF-02LS TSSLP-2-1

CRITICAL D4613 ESD0P2RF-02LS TSSLP-2-1

Left USB Port A

CRITICAL J4600 USB3.0-J44-ALT F-RT-TH

VBUS SSTX+ SSTX- GND D- D+ GND SSRX+ SSRX- GND

75 USB3_EXTA_R2D_P

75 USB3_EXTA_R2D_N

75 USB_LT1_N

75 USB_LT1_P

514-0934

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
USB 3.0 CONNECTORS

Apple Inc.

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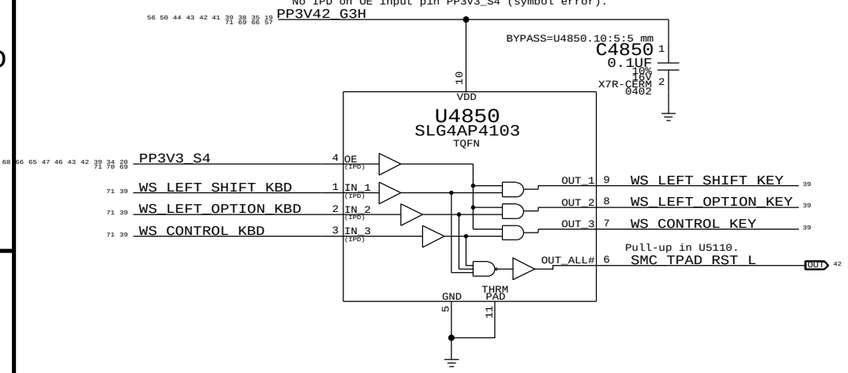
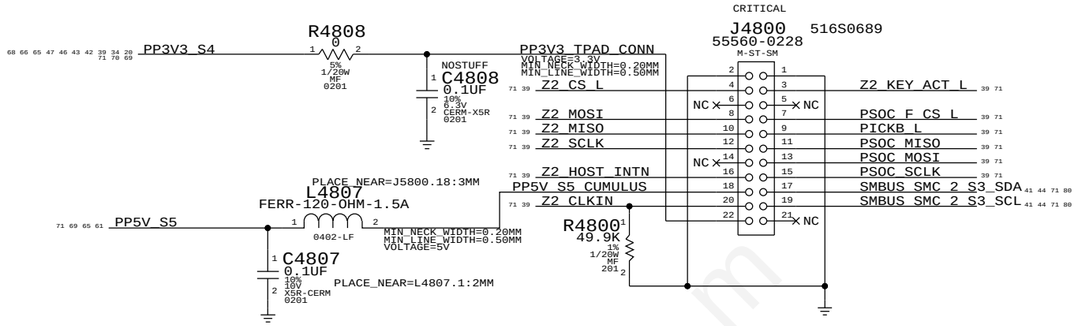
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

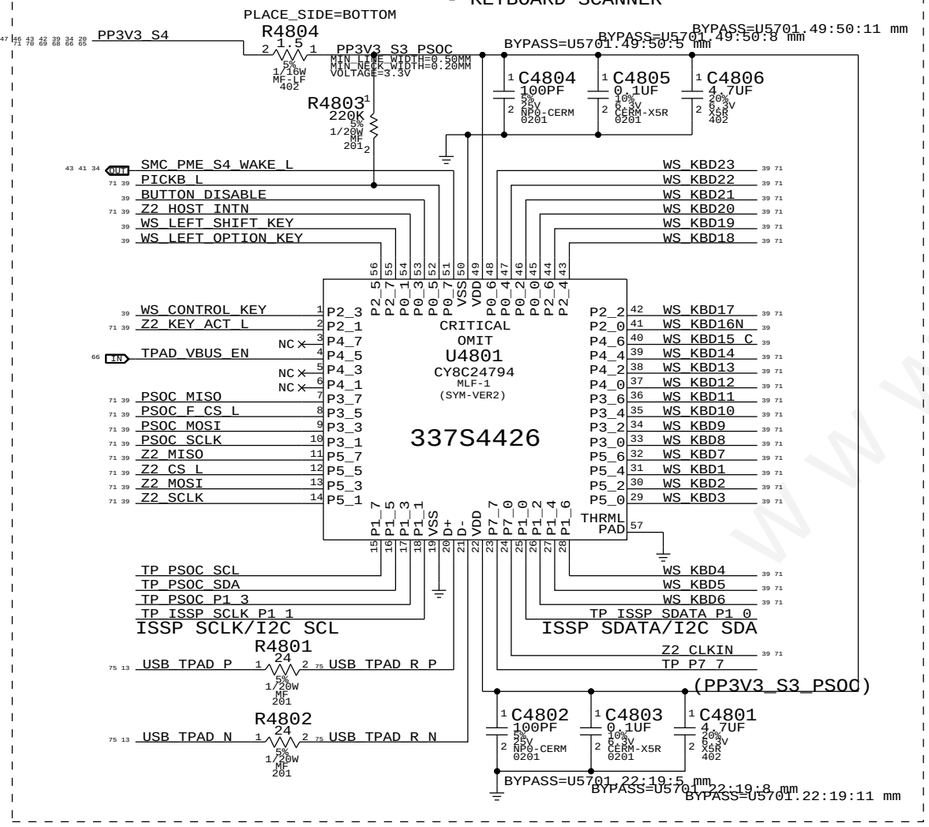


IPD Flex Connector



PSOC USB CONTROLLER

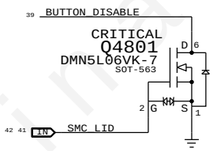
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



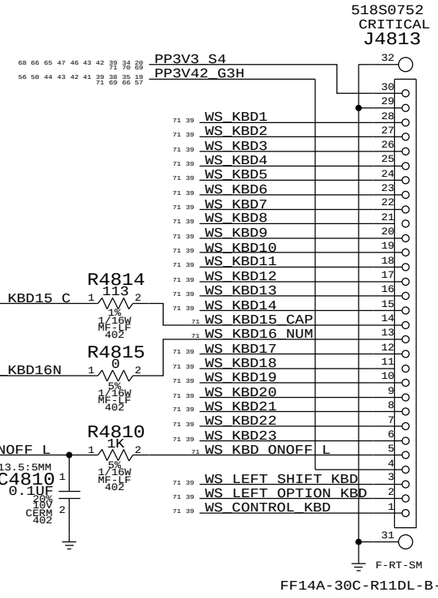
TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V



Keyboard Connector



FF14A-30C-R11DL-B-3H

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

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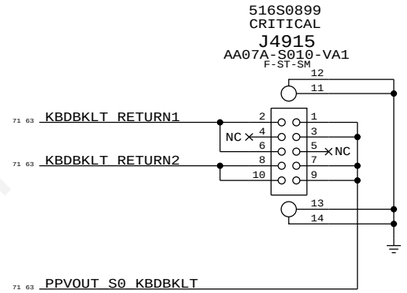
Keyboard Backlight Connector



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SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

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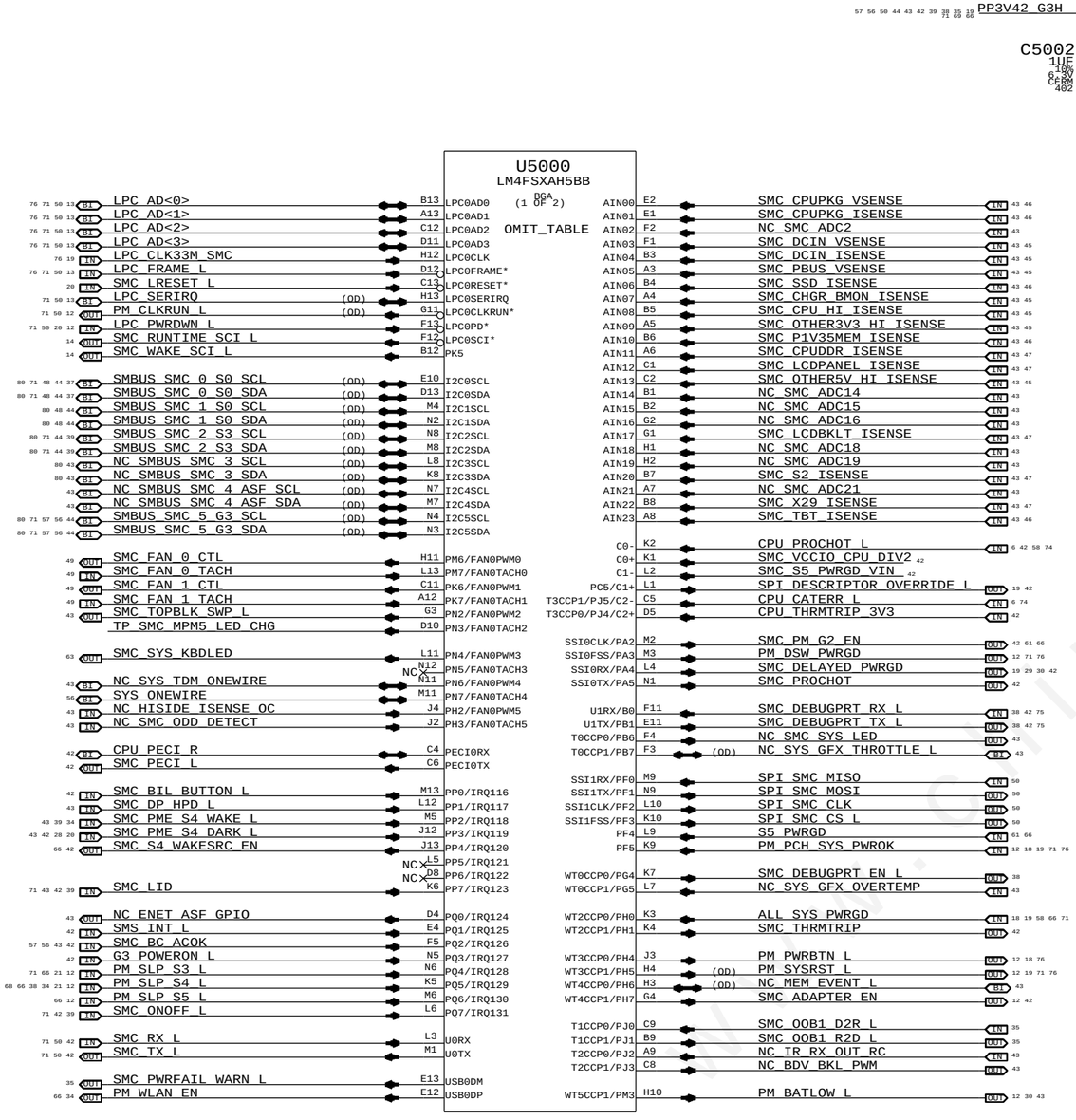
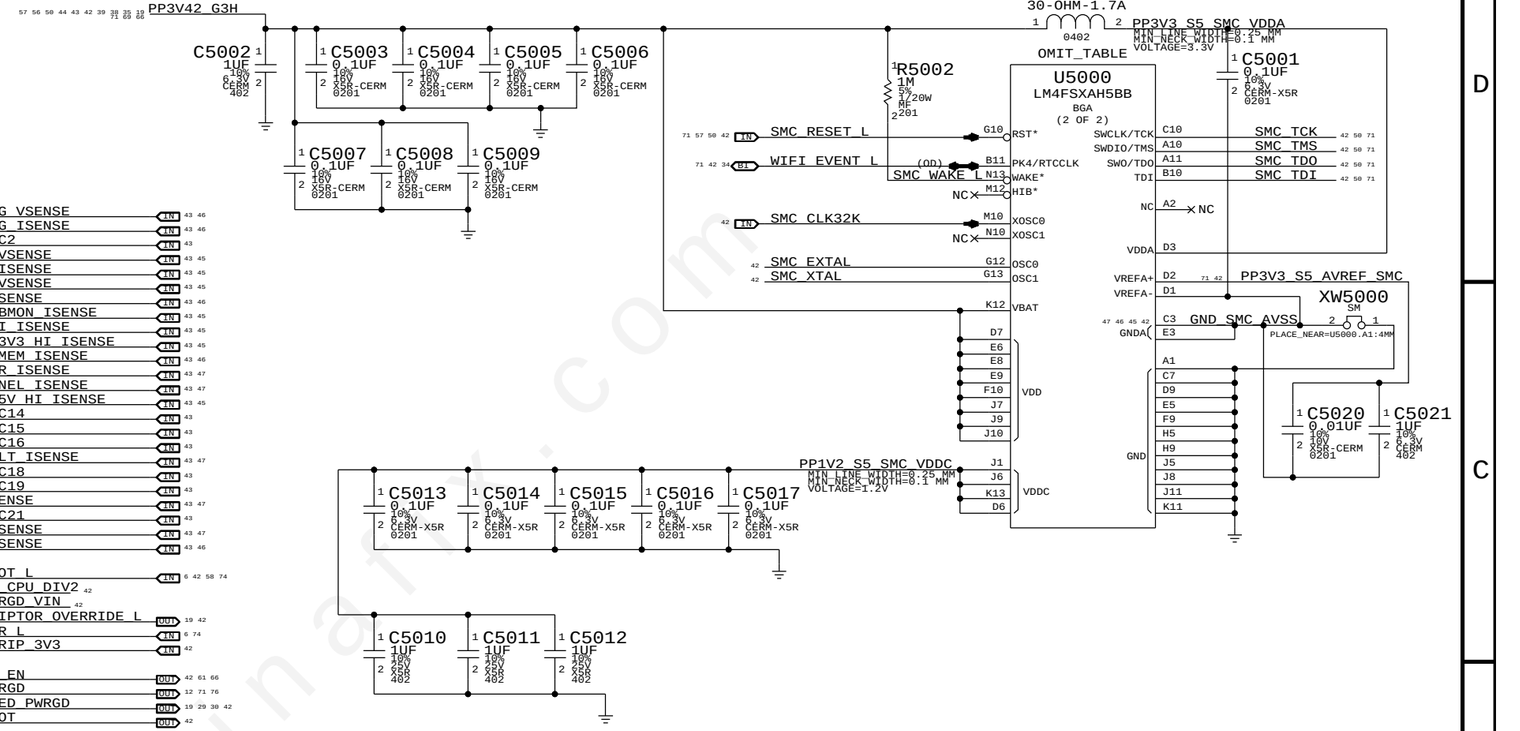
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CHANG_J45	SYNC_DATE=03/15/2013
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
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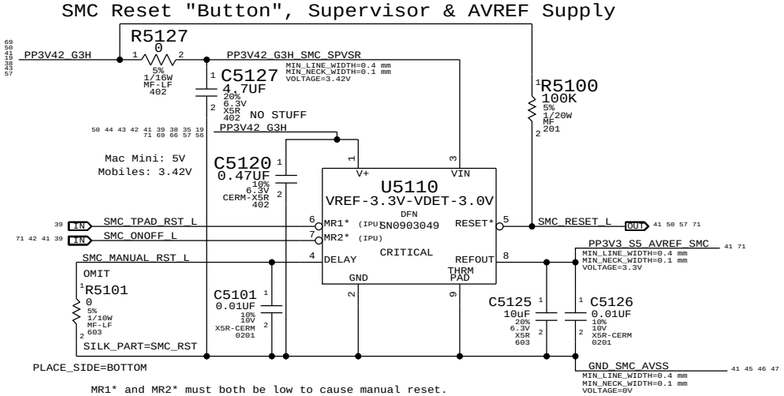
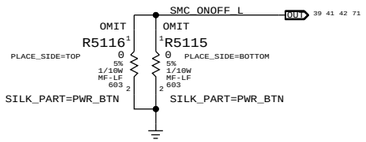
SMC Reset "Button", Supervisor & AVREF Supply



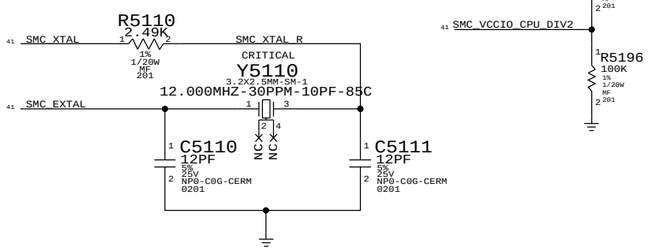
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

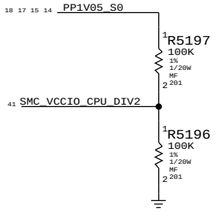
Debug Power "Buttons"



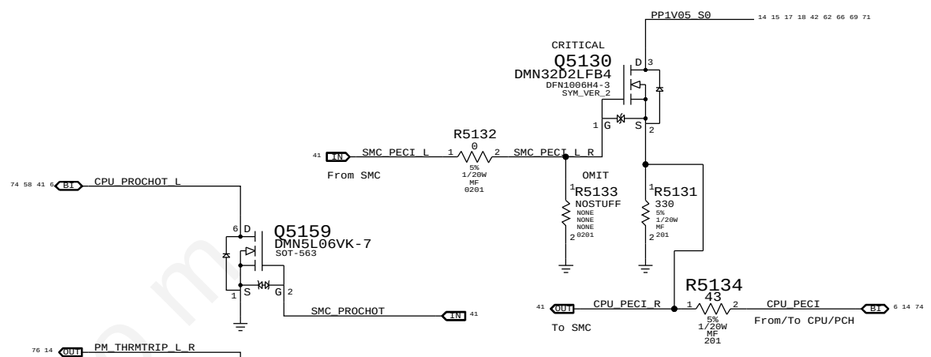
SMC Crystal Circuit

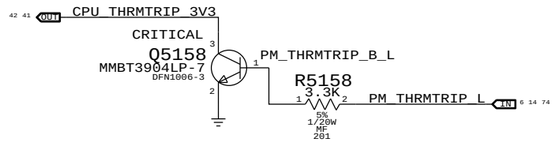


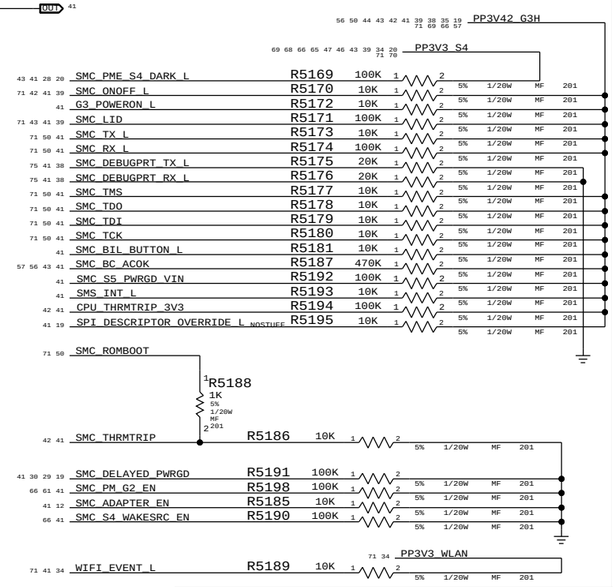
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ



SMC12 PECI SUPPORT







SYNC_MASTER=CHANG_J45 SYNC_DATE=11/12/2012

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Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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SMC_BC_ACOK — SMC_BC_ACOK (MAKE_BASE=TRUE)
NC_HISIDE_ISENSE_OC — NC_HISIDE_ISENSE_OC (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_CPUPKG_VSENSE — SMC_CPUPKG_VSENSE (MAKE_BASE=TRUE)
SMC_CPUPKG_ISENSE — SMC_CPUPKG_ISENSE (MAKE_BASE=TRUE)
NC_SMC_ADC2 — NC_SMC_ADC2 (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_DCIN_VSENSE — SMC_DCIN_VSENSE (MAKE_BASE=TRUE)
SMC_DCIN_ISENSE — SMC_DCIN_ISENSE (MAKE_BASE=TRUE)
SMC_PBUS_VSENSE — SMC_PBUS_VSENSE (MAKE_BASE=TRUE)
SMC_SSD_ISENSE — SMC_SSD_ISENSE (MAKE_BASE=TRUE)
SMC_CHGR_BMON_ISENSE — SMC_CHGR_BMON_ISENSE (MAKE_BASE=TRUE)
SMC_CPU_HI_ISENSE — SMC_CPU_HI_ISENSE (MAKE_BASE=TRUE)
SMC_OTHER3V3_HI_ISENSE — SMC_OTHER3V3_HI_ISENSE (MAKE_BASE=TRUE)
SMC_P1V35MEM_ISENSE — SMC_P1V35MEM_ISENSE (MAKE_BASE=TRUE)
SMC_CPUDDR_ISENSE — SMC_CPUDDR_ISENSE (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_LCDPANEL_ISENSE — SMC_LCDPANEL_ISENSE (MAKE_BASE=TRUE)
SMC_OTHER5V_HI_ISENSE — SMC_OTHER5V_HI_ISENSE (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_ADC14 — NC_SMC_ADC14 (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_ADC15 — NC_SMC_ADC15 (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_ADC16 — NC_SMC_ADC16 (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_LCDBKLT_ISENSE — SMC_LCDBKLT_ISENSE (MAKE_BASE=TRUE)
NC_SMC_ADC18 — NC_SMC_ADC18 (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_ADC19 — NC_SMC_ADC19 (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_S2_ISENSE — SMC_S2_ISENSE (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_ADC21 — NC_SMC_ADC21 (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_X29_ISENSE — SMC_X29_ISENSE (MAKE_BASE=TRUE)
SMC_TBT_ISENSE — SMC_TBT_ISENSE (MAKE_BASE=TRUE)
NC_SMBUS_SMC_4_ASF_SCL — NC_SMBUS_SMC_4_ASF_SCL (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_4_ASF_SDA — NC_SMBUS_SMC_4_ASF_SDA (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_3_SCL — NC_SMBUS_SMC_3_SCL (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_3_SDA — NC_SMBUS_SMC_3_SDA (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_BDV_BKL_PWM — NC_BDV_BKL_PWM (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_PME_S4_DARK_L (MAKE_BASE=TRUE) — SMC_PME_S4_DARK_L
SMC_PME_S4_DARK_L

NC_ENET_ASF_GPIO — NC_ENET_ASF_GPIO (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_SYS_LED — NC_SMC_SYS_LED (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_MEM_EVENT_L — NC_MEM_EVENT_L (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_ODD_DETECT — NC_SMC_ODD_DETECT (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_IR_RX_OUT_RC — NC_IR_RX_OUT_RC (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_TDM_ONEWIRE — NC_SYS_TDM_ONEWIRE (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_GFX_THROTTLE_L — NC_SYS_GFX_THROTTLE_L (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_GFX_OVERTEMP — NC_SYS_GFX_OVERTEMP (MAKE_BASE=TRUE NO_TEST=TRUE)

Spare S4 IRQ

PP3V3_S4 — R5259 100K 5% 1/20W MF 201 — SMC_DP_HPD_L (OUT)

Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99
SM
NC, NC, PP3V42_G3H, SMC_LID_R, NC, NC
R5250 0 5% 1/20W MF 0201
SMC_LID
C5250 0.001UF 10% 50V X7R-CERM 0402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

PP3V3_S4 — R5282 100K 5% 1/20W MF 201
SMC_PME_S4_WAKE_L (IN) — SMC_PME_S4_WAKE_L (MAKE_BASE=TRUE) (OUT)
SMC_PME_S4_WAKE_L (IN)

SMC_TOPBLK_SWP_L (IN) — R5283 1K 5% 1/20W MF 201 — PCH_STRP_TOPBLK_SWP_L (OUT)

PM_BATLOW_L (IN) — PM_BATLOW_L (MAKE_BASE=TRUE) (OUT)

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Apple Inc.
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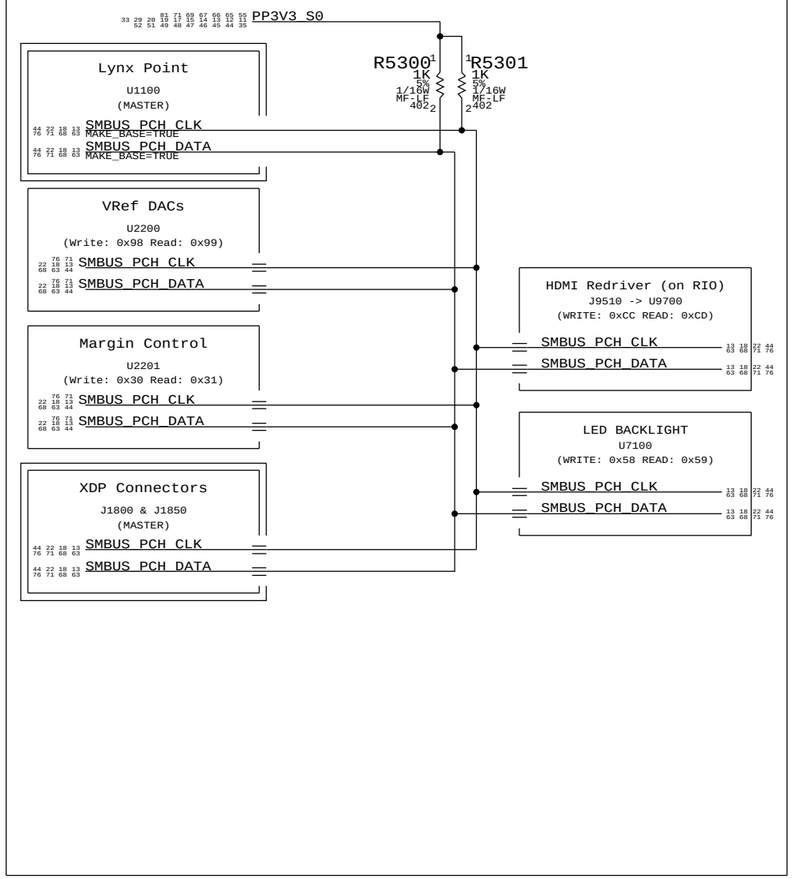
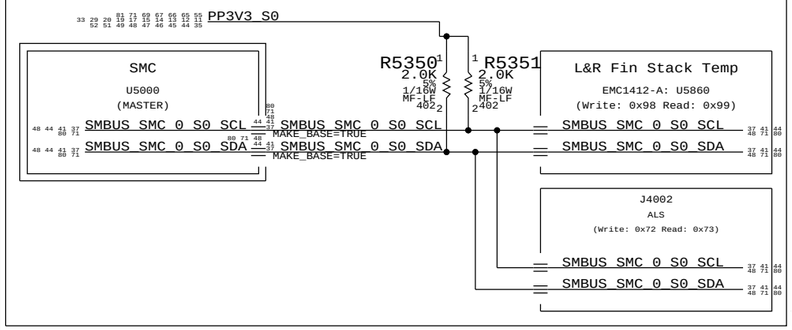
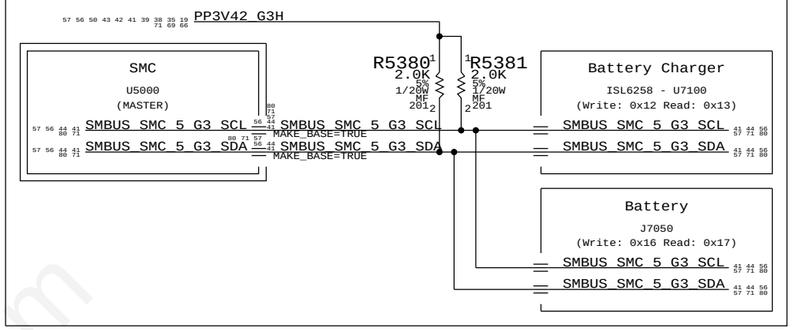
PCH SMBus "0" Connections



SMC "0" SMBus Connections

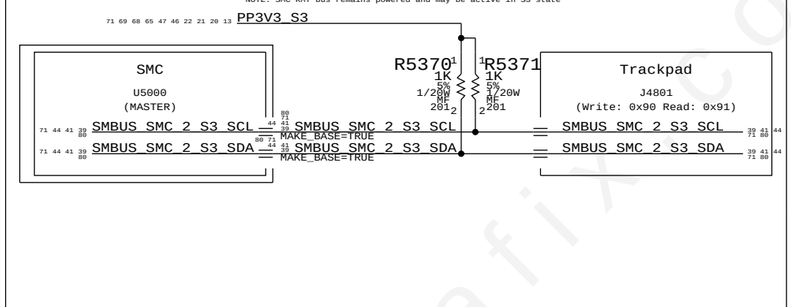


SMC "5" SMBUS CONNECTIONS



SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state



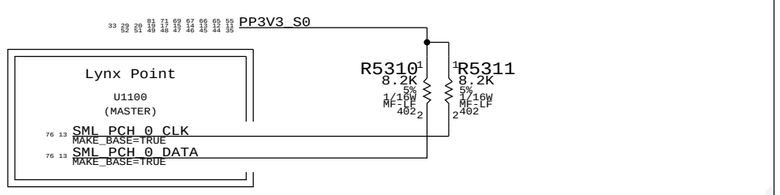
SMC "4" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

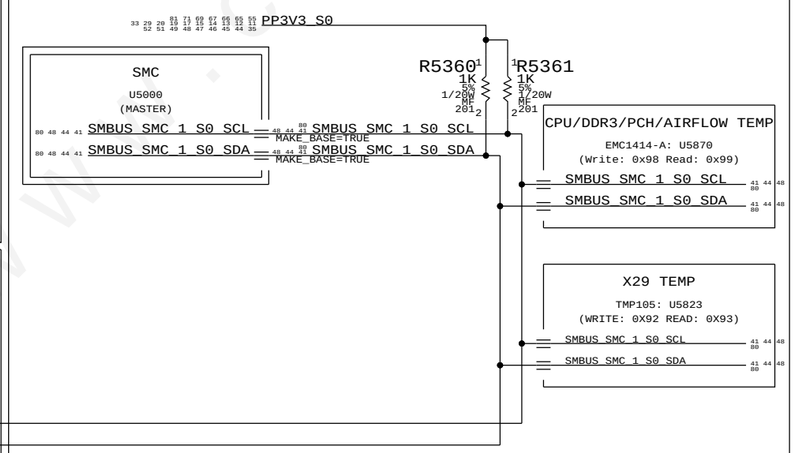
SMC "3" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

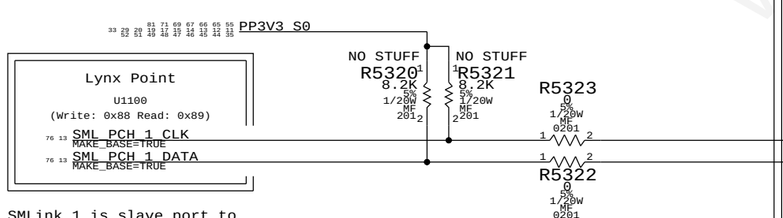
PCH "SMLink 0" Connections



SMC "1" SMBUS CONNECTIONS



PCH "SMLink 1" Connections



SMLink 1 is slave port to access PCH & CPU via PECI.

SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE: SMBus Connections

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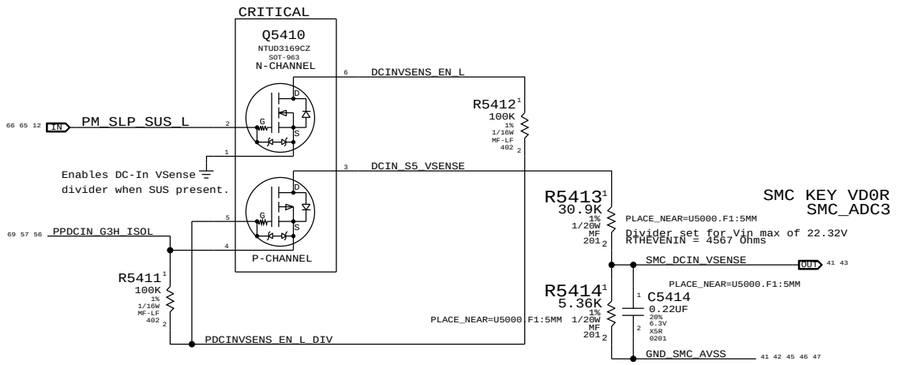
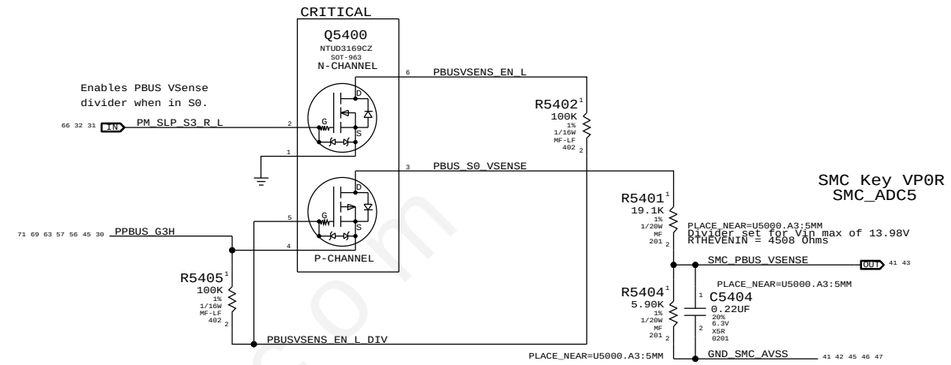
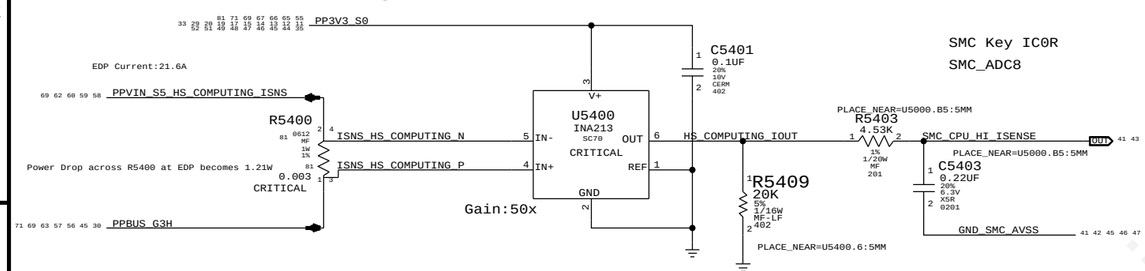
DC-In Voltage Sense Enable & Filter



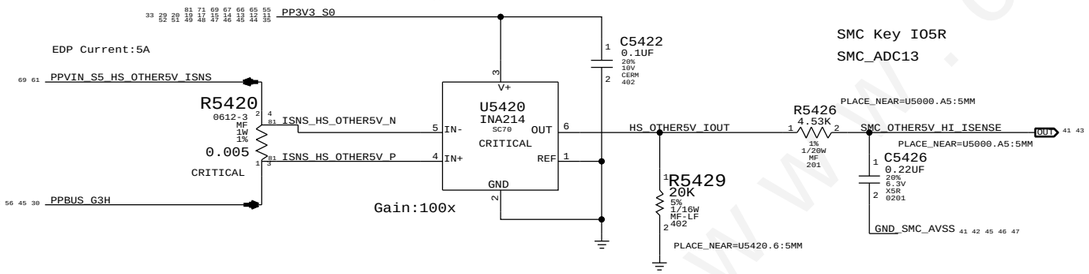
PBUS Voltage Sense Enable & Filter



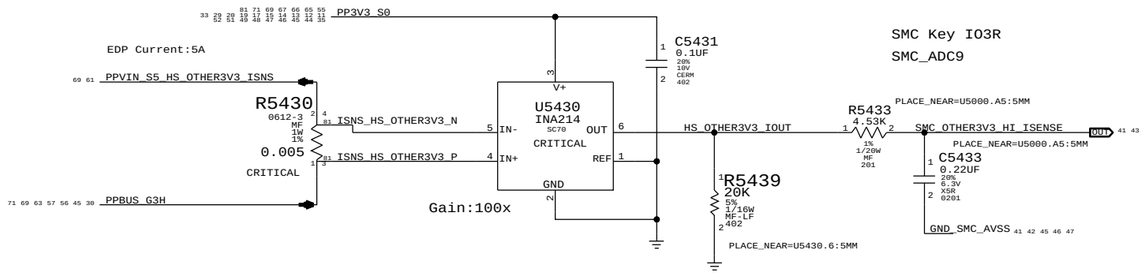
COMPUTING High Side Current Sense / Filter



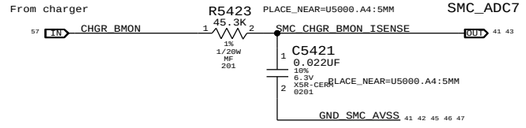
OTHERS (5V) High Side Current Sense / Filter



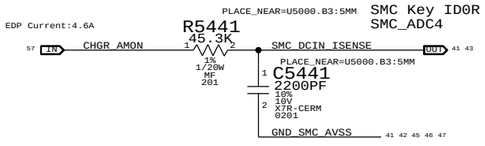
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CHANG_J45 SYNC_DATE=12/21/2012

PAGE TITLE: High Side Voltage and Current Sensing

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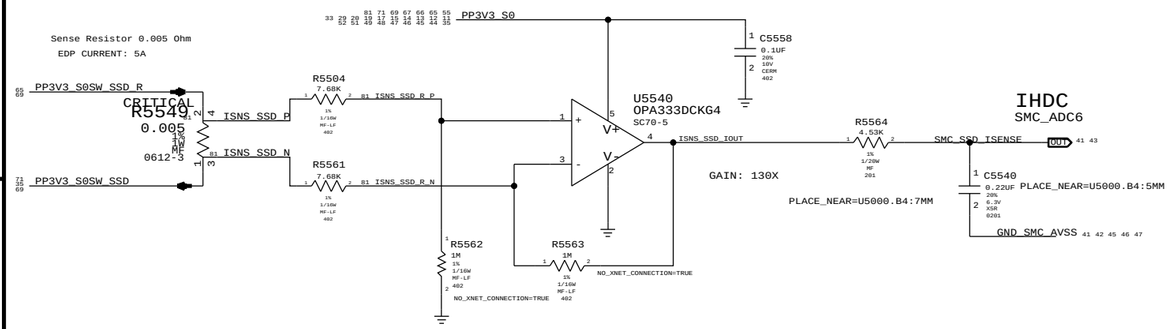
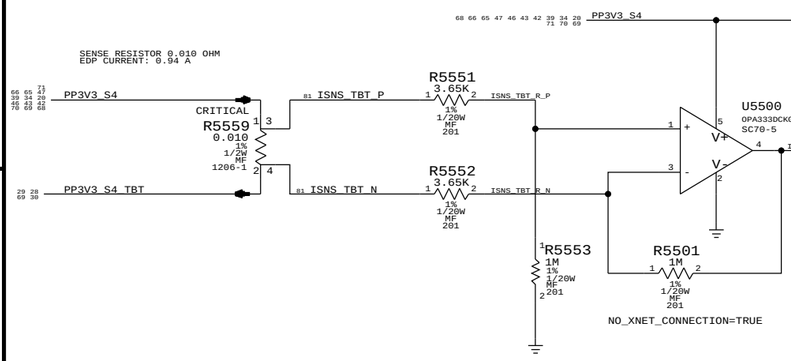
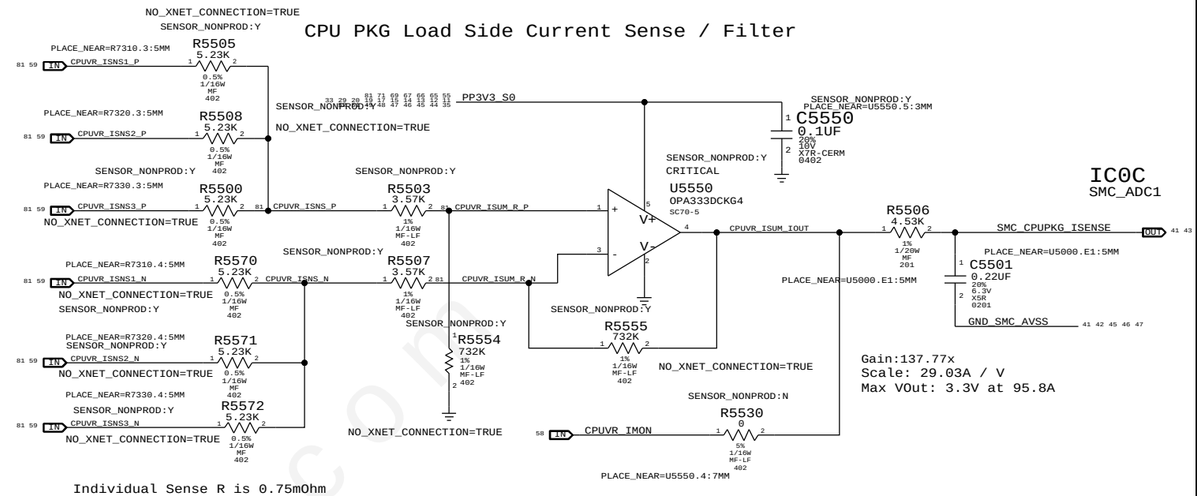
SSD CURRENT SENSE



TBT Router CURRENT SENSE

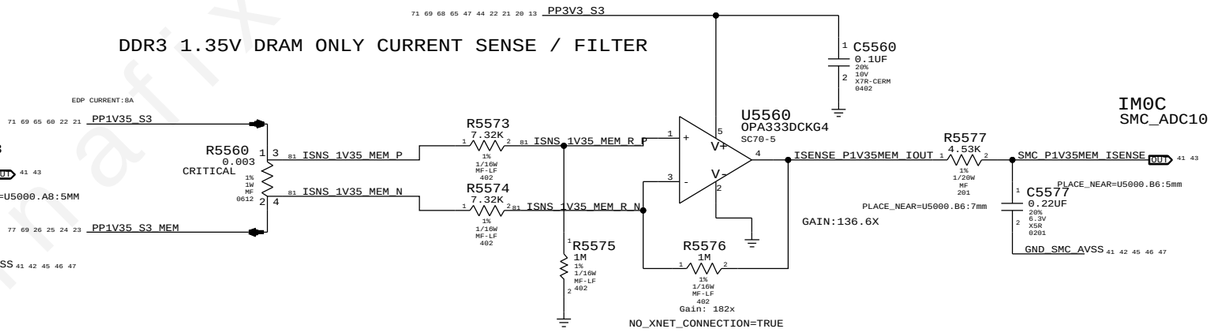


CPU PKG Load Side Current Sense / Filter

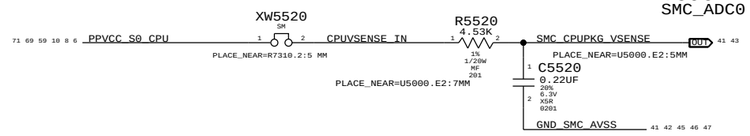


Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER



CPU Vcore Voltage Sense / Filter



SYNC_MASTER=CHANG_J45	SYNC_DATE=03/15/2013
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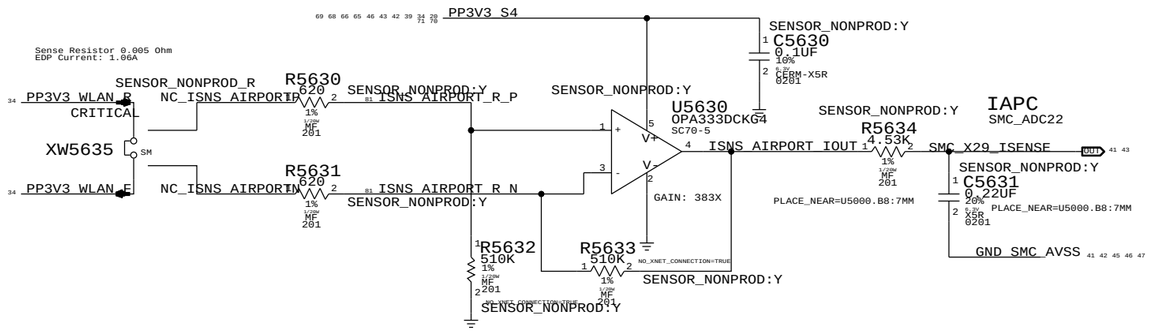
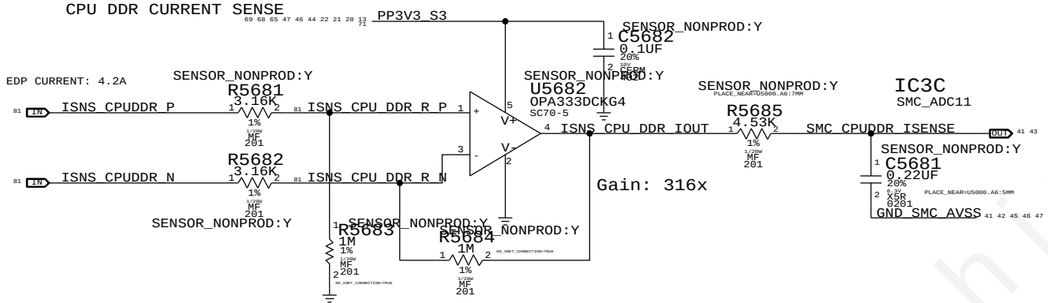
X29 AIRPORT CURRENT SENSE

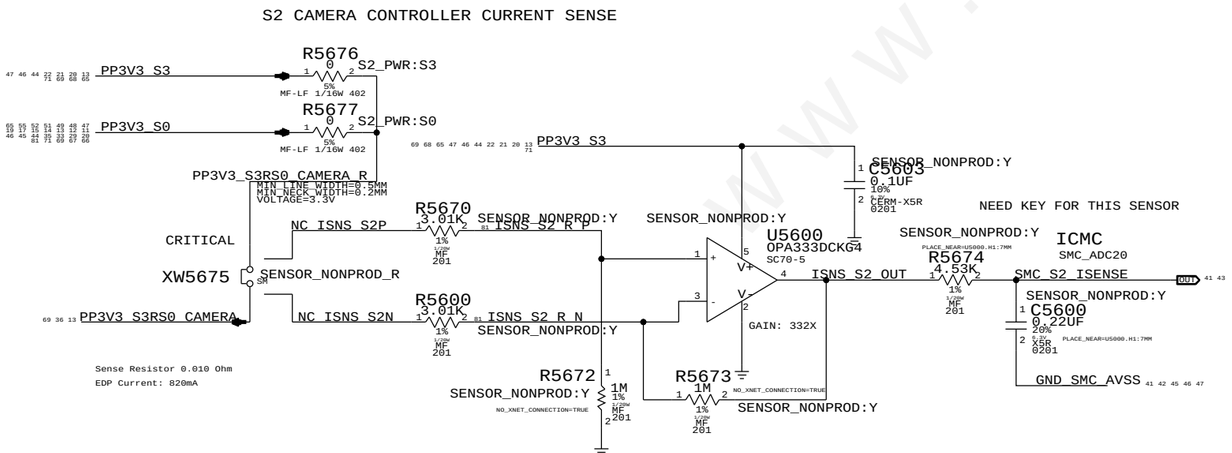


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5600,C5631,C5660,C5681,C5671,C5610		SENSOR_NONPROD:N

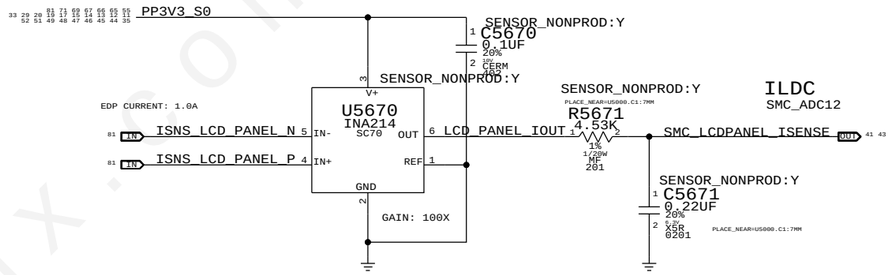
CPU DDR CURRENT SENSE



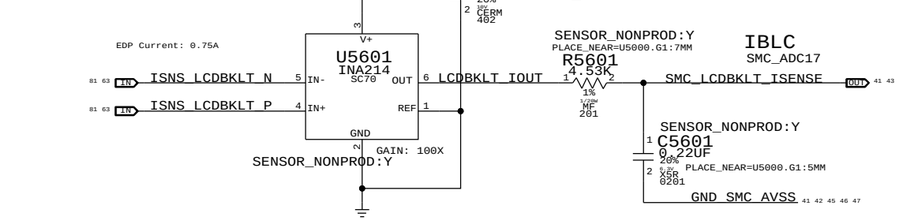
S2 CAMERA CONTROLLER CURRENT SENSE



LCD PANEL CURRENT SENSE



LCD BKLT Current Sense



SYNC_MASTER=CHANG_J45 SYNC_DATE=12/21/2012

PAGE TITLE: Debug Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 56 OF 118

SHEET: 47 OF 81

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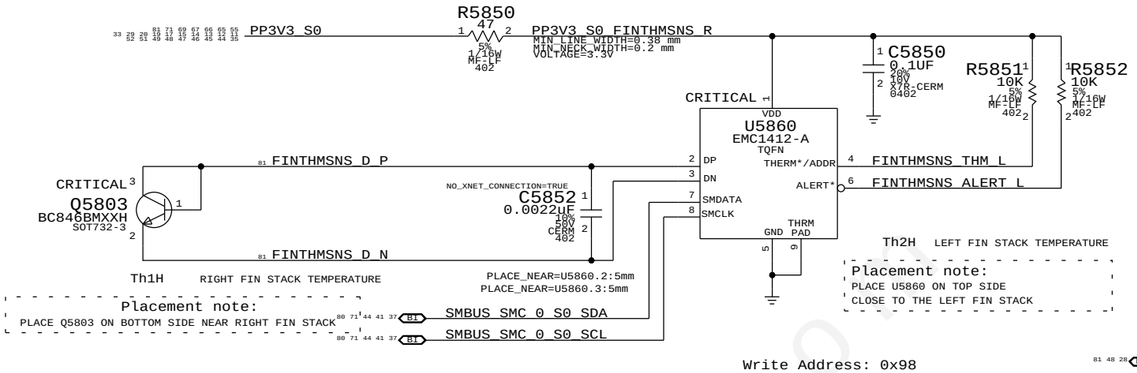
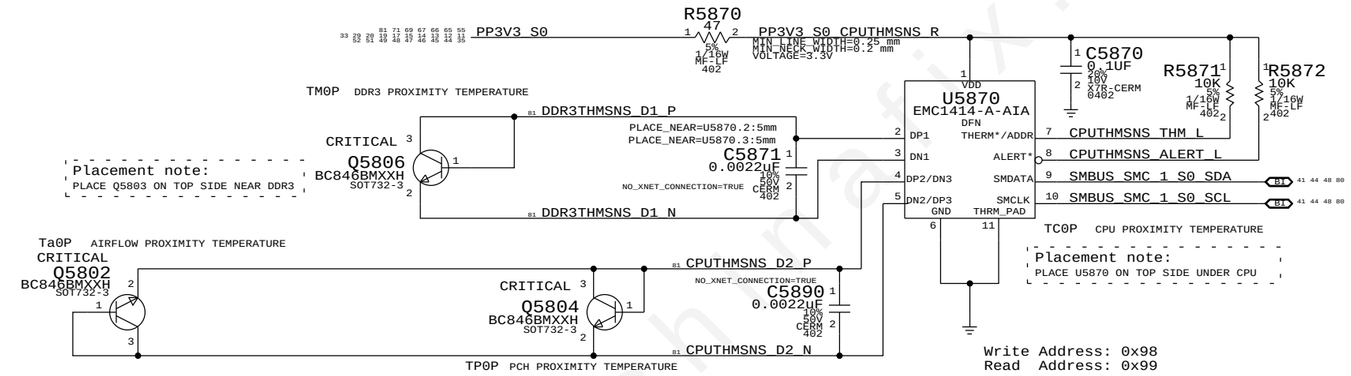
LEFT FIN STACK/RIGHT FIN STACK



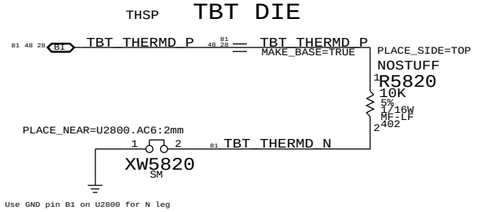
Write Address: 0x98
Read Address: 0x99

DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY

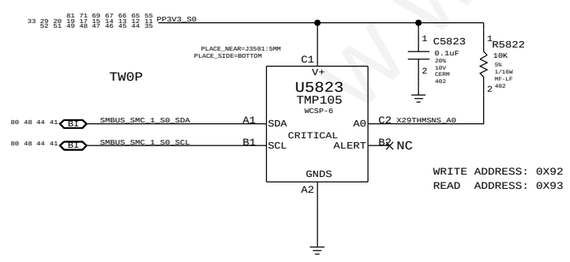


Write Address: 0x98
Read Address: 0x99

TBT DIE



X29 PROXIMITY



WRITE ADDRESS: 0X92
READ ADDRESS: 0X93

SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 58 OF 118
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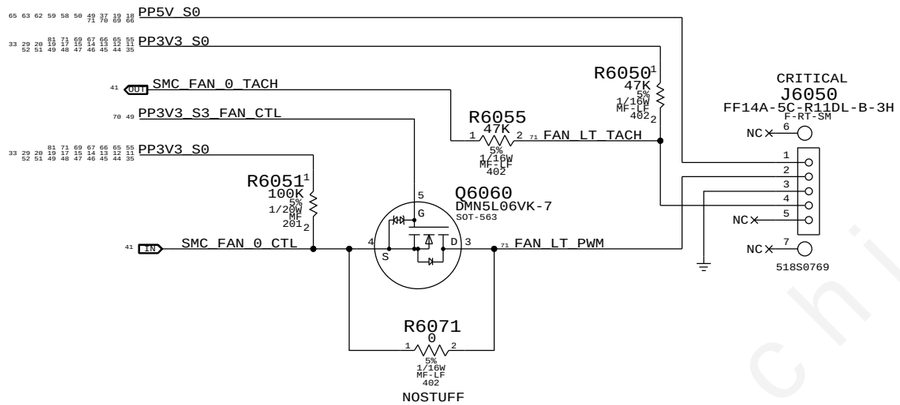
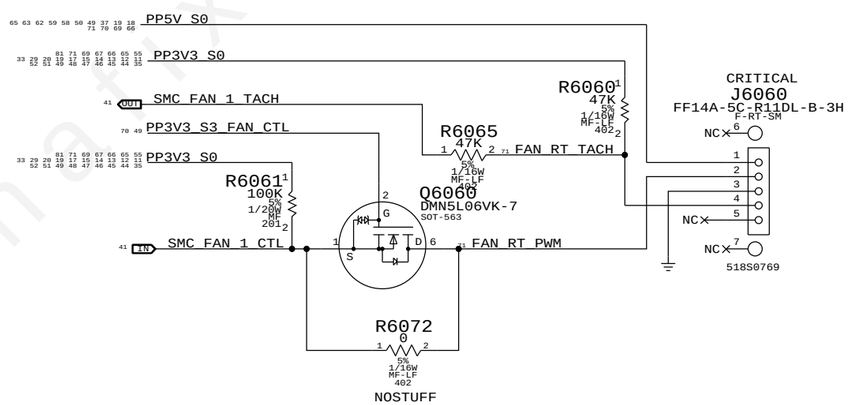
Left Fan



Right Fan



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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 60 OF 118

SHEET: 49 OF 81

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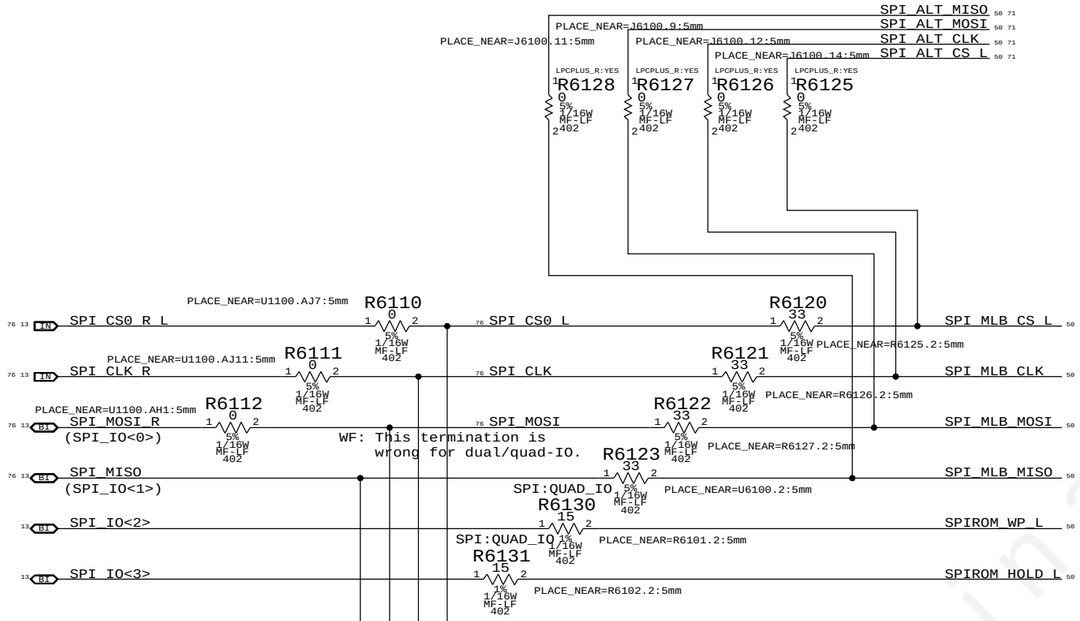
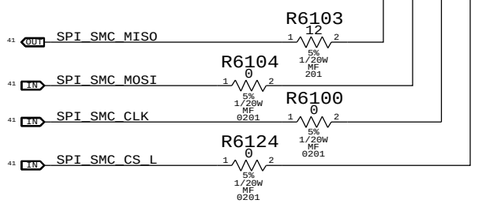
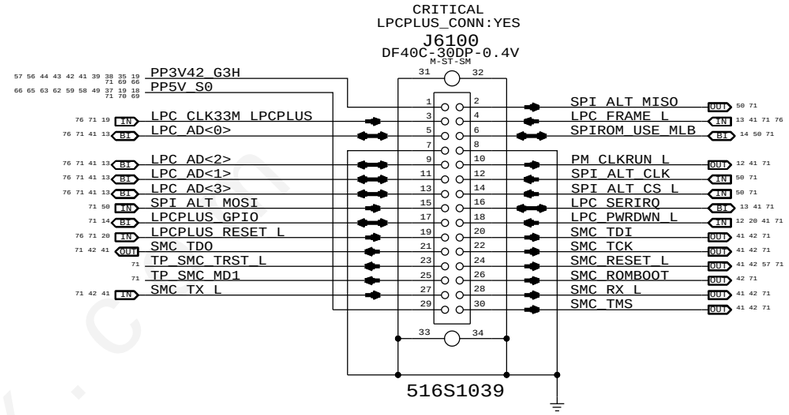
SPI Bus Series Termination



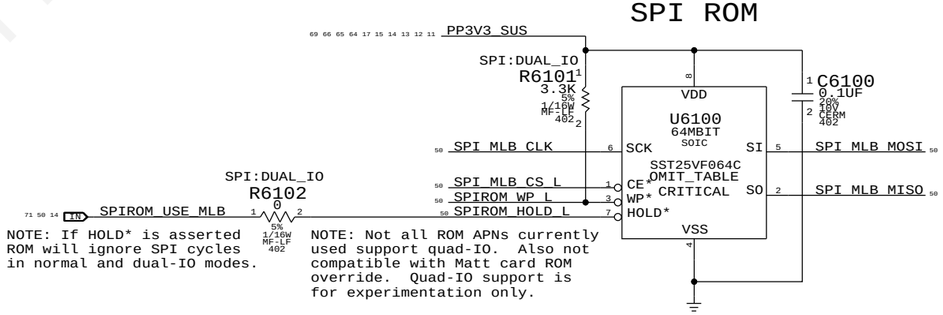
SMC12 SPI SUPPORT



LPC+SPI Connector



SPI ROM



NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and dual-IO modes.

NOTE: Not all ROM APNs currently used support quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: SPI ROM / LPC+SPI Conn.

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 61 OF 118

SHEET: 50 OF 81

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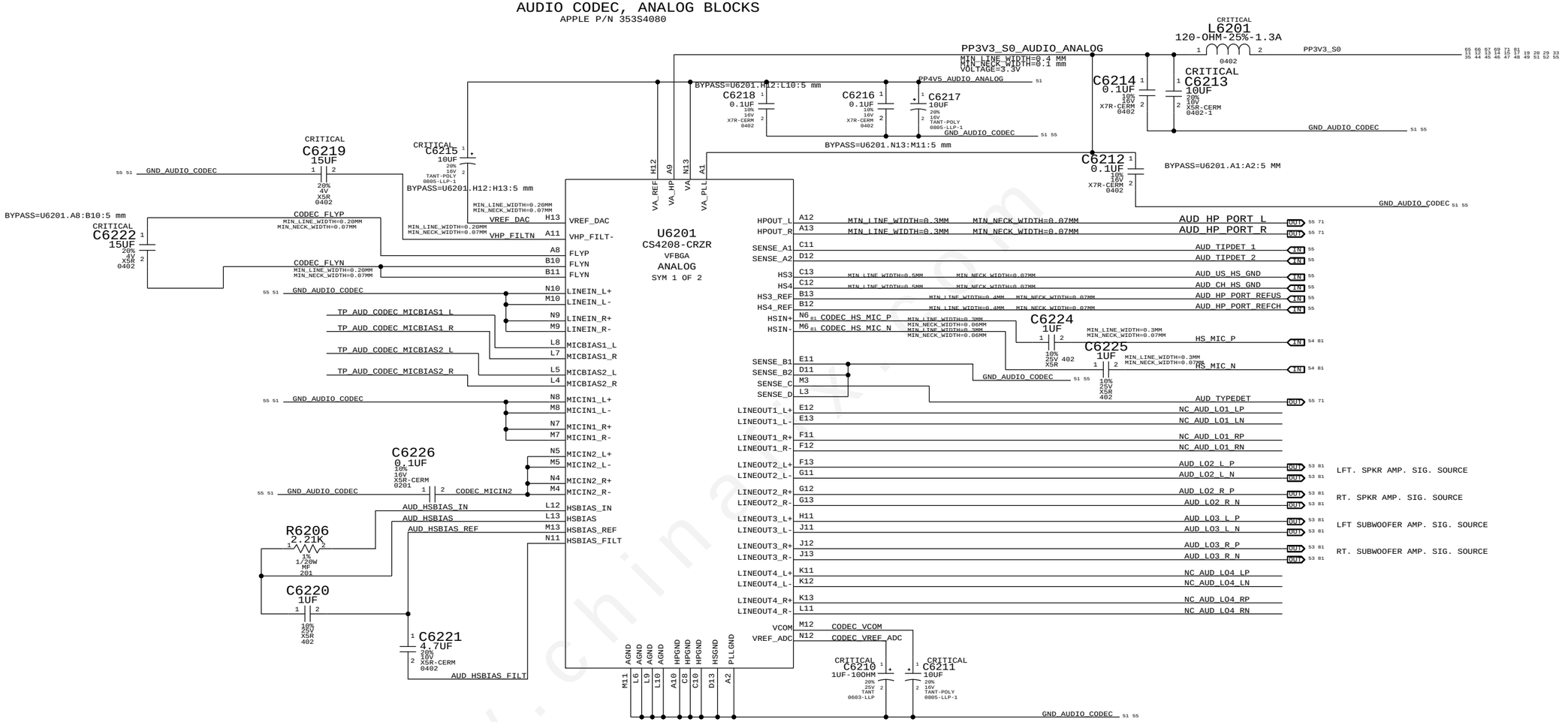
AUDIO CODEC, ANALOG BLOCKS

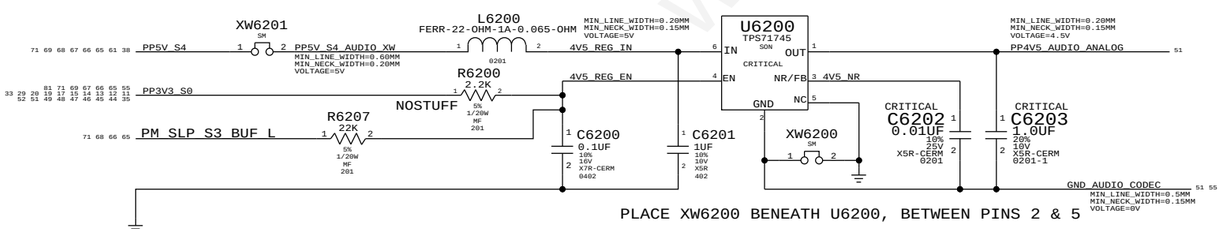
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

SYNC_MASTER=J0E_J45	SYNC_DATE=07/30/2013
PAGE TITLE	AUDIO:CODEC, ANALOG
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 62 OF 118
	SHEET 51 OF 81

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AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

L6300
FERR-22-OHM-1A-0.065-OHM

PP1V5_S0 → C6300 4.7UF 20% 4V X5R-1 402 → C6301 0.1UF 10% 16V X7R-CERM 0201
PP1V5_S0_AUDIO_DIG
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.07MM
VOLTAGE=1.5V
BYPASS=U6201.J2:J1:5 mm

C6302 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.E1:F1:5 mm

PP3V3_S0
R6324 100K 5% 1/20W MF 201
R6325 100K 5% 1/20W MF 201

R6323 100K 5% 1/20W MF 201 NOSTUFF
R6322 100K 5% 1/20W MF 201

GPIO0_SPKR_SHUTDOWN
PD_CS4208_GPIO1
SPKRCONN_L_ID
SPKRCONN_R_ID
DFET_OPENUS
DFET_OPENCH

R6331 22 5% 1/20W MF 201

HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L

NC_CS4208_MCLKA
NC_CS4208_SCLKA
NC_CS4208_LRCLKA
NC_CS4208_SDOUTA
NC_CS4208_MCLKB
NC_CS4208_SCLKB
NC_CS4208_LRCLKB
NC_CS4208_SDOUTB

BYPASS=U6201.G1:F1:5 mm
C6303 0.1UF 10% 6.3V CERM-XSR 0201
BYPASS=U6201.K1:K3:5 mm
C6304 0.1UF 10% 6.3V CERM-XSR 0201
C6305 10UF 20% 10V X5R-CERM 0402-1

PP3V3_S0
C6306 10UF 20% 10V X5R-CERM 0402-1
BYPASS=U6201.A7:E3:5 mm
C6307 0.1UF 10% 6.3V CERM-XSR 0201

OMIT
R6302 SHORT 402

U6201
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2

H3	GPIO0	
H2	GPIO1	
H1	GPIO2	
C4	GPIO3	
C5	GPIO4	
C7	GPIO5	
C9	GPO0	NC_CS4208_GPO0
B9	GPO1	NC_CS4208_GPO1
F2	BCLK	
E2	SYNC	
D1	SDI0	
C1	SDI1	TP_CS4208_HDA_SDOUT1
D2	SDO0	
C2	SDO1	
C3	SDO2	
B1	SDO3	
D3	RST*	
A5	MCLK_A	
B2	SCLK_A	
B4	LRCK_A	
A3	SDOUT_A	
B3	SDIN_A	
A6	MCLK_B	
B6	SCLK_B	
B5	LRCK_B	
B8	SDOUT_B	
A4	SDIN_B	
C6	SDA	
B7	SCL	
J1	DGND	
F1	LGND	
E3	LGND	
F3	LGND	
J3	LGND	
K3	LGND	
J2	VD	
E1	VL_HD	
A7	VL_SP	
G1	VL_IF	
K1	VL_DM	
G3	SPDIF_IN	CS4208_SPDIF_IN
G2	SPDIF_OUT	CS4208_SPDIF_OUT
N3	DMIC_SDA0	
N2	DMIC_SCL0	NC_DMIC_CLK0
N1	DMIC_SDA1	
M1	DMIC_SCL1	NC_DMIC_CLK1
M2	DMIC_SDA2	
L1	DMIC_SCL2	NC_DMIC_CLK2
K2	DMIC_SDA3	
L2	DMIC_SCL3	
F6	NC	
F7	NC	
F8	NC	
G6	NC	
G7	NC	
G8	NC	
H6	NC	
H7	NC	
H8	NC	

R6330 33 1% 1/10W MF-LF 402 SPDIF_OUT_JACK
R6332 75 1% 1/10W MF-LF 402 DMIC_CLK3_R → DMIC_CLK3
DMIC_SDA3

PP6301 P3MMSM PP — DMIC_SDA3 — PLACE_NEAR=U6201.N3:5 mm
PP6302 P3MMSM PP — HDA_BIT_CLK — PLACE_NEAR=U6201.F2:5 mm
PP6303 P3MMSM PP — HDA_SYNC — PLACE_NEAR=U6201.E2:5 mm
PP6304 P3MMSM PP — HDA_SDOUT — PLACE_NEAR=U6201.D2:5 mm
PP6305 P3MMSM PP — CS4208_HDA_SDOUT0_R — PLACE_NEAR=U6201.D1:5 mm

SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013
PAGE TITLE: AUDIO:CODEC, DIGITAL
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 63 OF 118
SHEET: 52 OF 81

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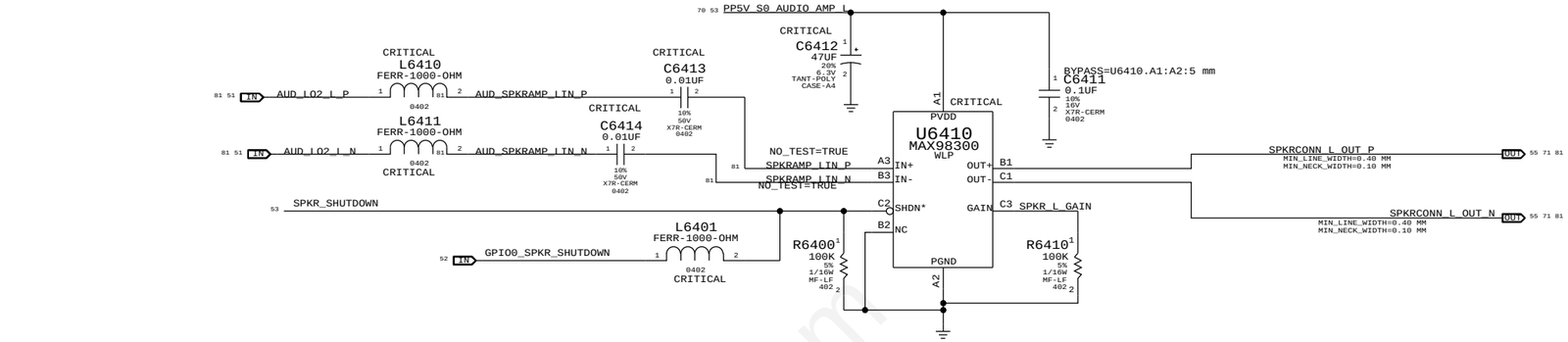
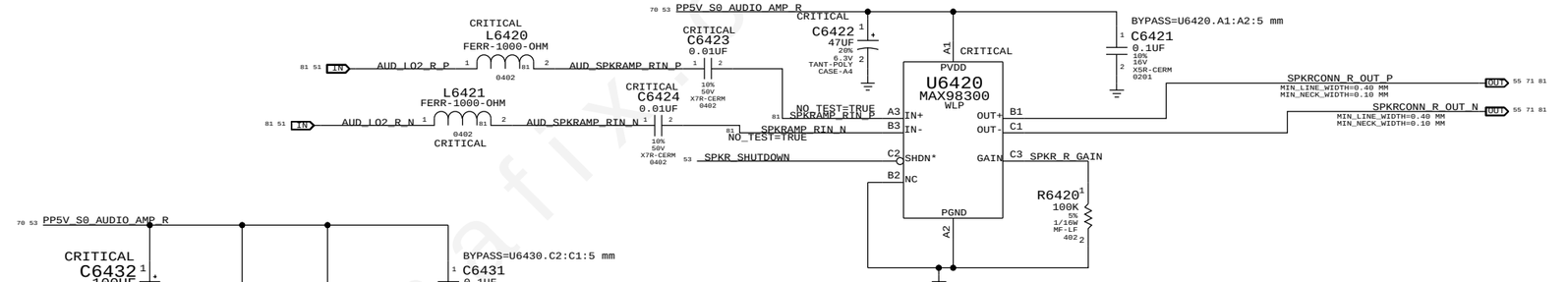
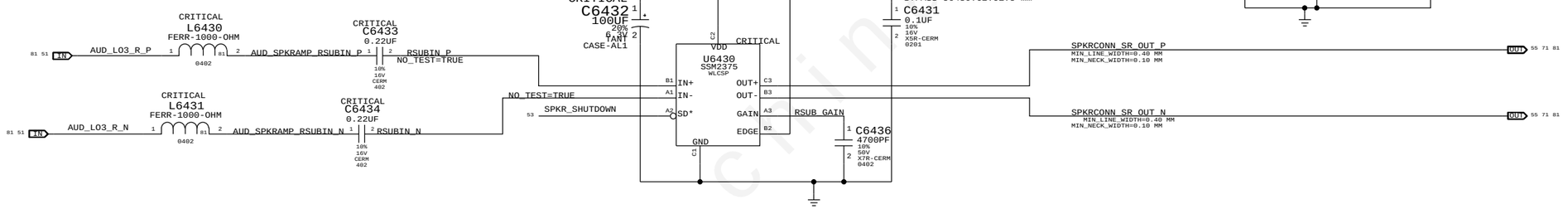
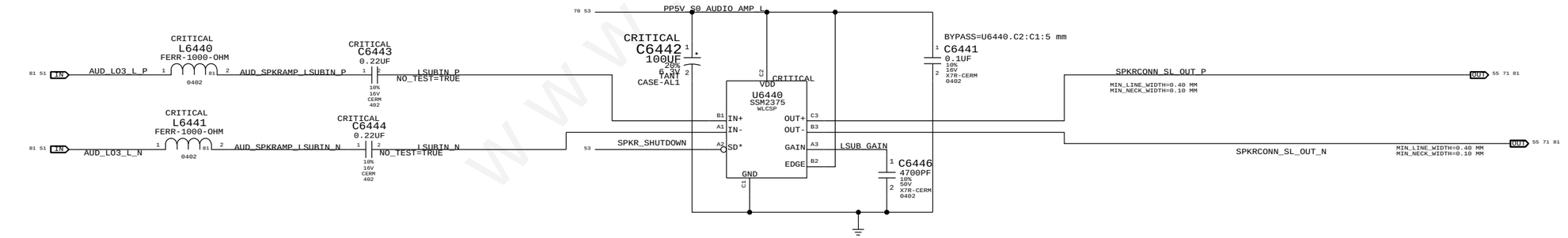
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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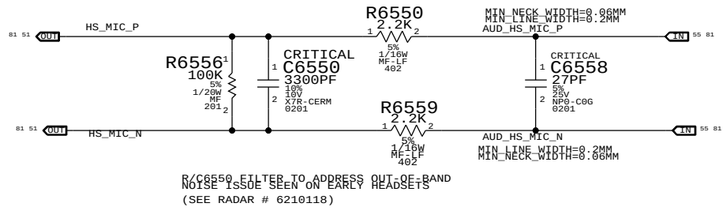

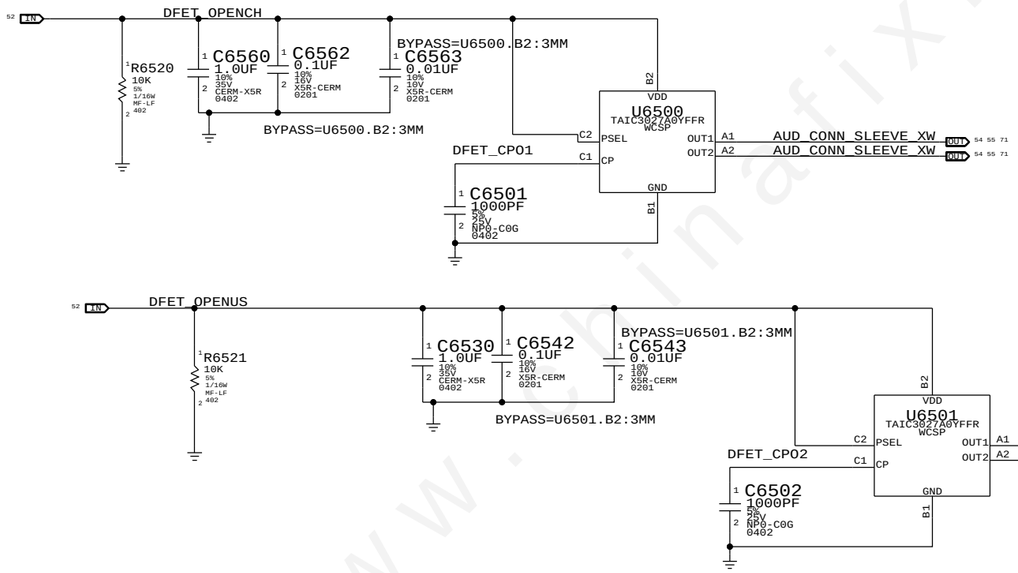

SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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SHEET: 54 OF 81

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

PP3V3_S0
DMIC_SDA3
DMIC_CLK3
OMIT
R6680
SHORT
DMIC_SDA2

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

MIC
AUDIO GND
2RTN
DET2
DET1
1RTN
R.AUDIO
AUDIO GND
AUDIO
NC
VIN
VDD
GND
OPERATING VOLTAGE 3.3
POF
SHELL PINS

L6611 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFCH
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM

XW6600 SM PLACE_NEAR=J6600.3:2.54mm

L6612 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CH_HS_GND
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM

XW6601 SM
AUD_HS_MIC_P

L6613 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFUS
AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM

XW6602 SM PLACE_NEAR=J6600.5:2.54mm

L6614 120-OHM-25%-1.3A 0402 CRITICAL
AUD_US_HS_GND
AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM

XW6603 SM
AUD_HS_MIC_N

L6604 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM

R6602 2.2K 5% 1/20W MF 201
L6608 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_2
AUD_CONN_TIPDET_2

GND_AUDIO_CODEC

R6603 2.2K 5% 1/20W MF 201
L6607 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_1
AUD_CONN_TIPDET_1

L6605 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM

L6606 FERR-470-OHM 0201 CRITICAL
AUD_TYPEDET
AUD_CONN_TYPEDET

SPDIF_OUT_JACK
PP3V3_S0

R6601 10K 5% 1/16W MF-LF 402

C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 6.3V CERM-X5R 0201

C6602 100PF 5% 25V NP0-CERM 0201
C6603 100PF 5% 25V NP0-CERM 0201
C6604 100PF 5% 25V NP0-CERM 0201
C6605 100PF 5% 25V NP0-CERM 0201
C6606 100PF 5% 25V NP0-CERM 0201
C6607 100PF 5% 25V NP0-CERM 0201
C6608 100PF 5% 25V NP0-CERM 0201

DZ6601 ESDALC5-1BM2 SOD882 CRITICAL
DZ6602 ESDALC5-1BM2 SOD882 CRITICAL
DZ6603 ESDALC5-1BM2 SOD882 CRITICAL
DZ6604 ESDALC5-1BM2 SOD882 CRITICAL
DZ6605 ESDALC5-1BM2 SOD882 CRITICAL
DZ6606 ESDALC5-1BM2 SOD882 CRITICAL
DZ6607 ESDALC5-1BM2 SOD882 CRITICAL

SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013
PAGE TITLE
AUDIO: JACK TRANSLATORS

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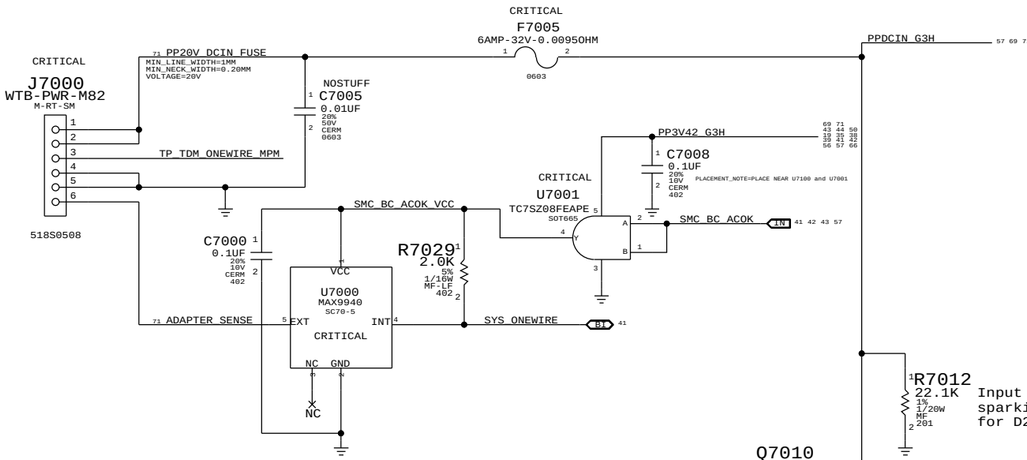
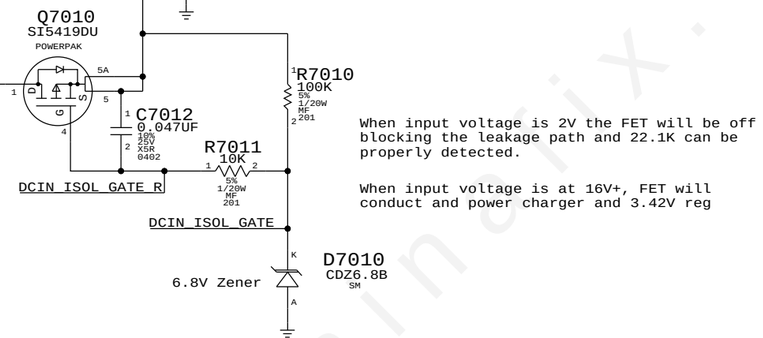
MagSafe DC Power Jack



1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.



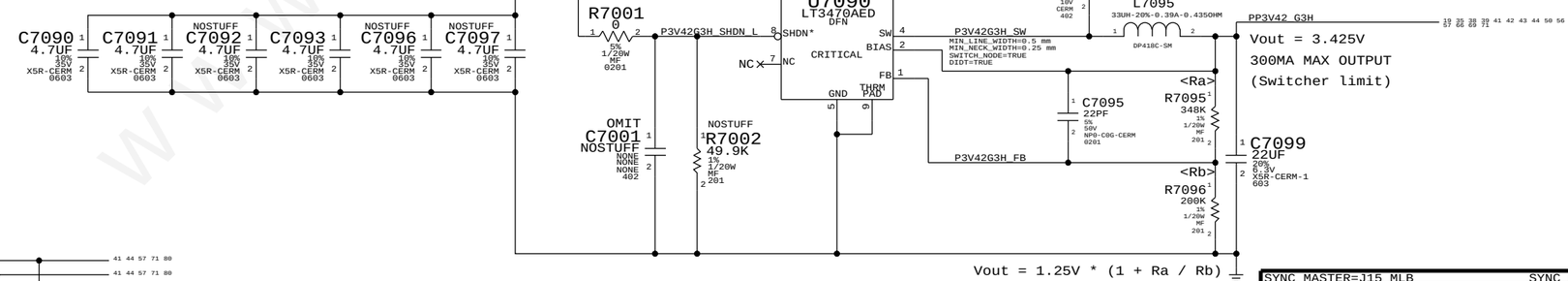
When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

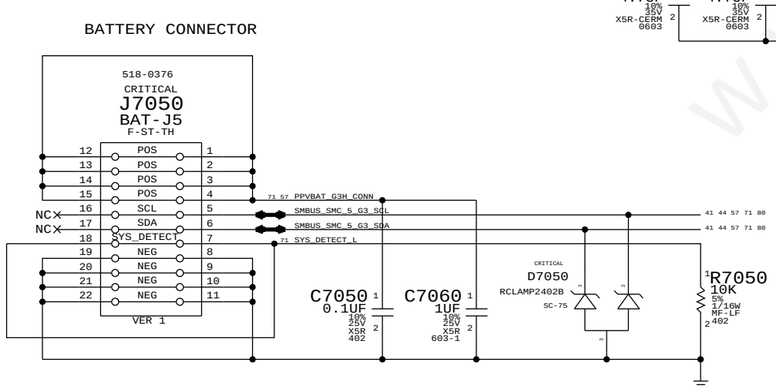
APN:353S3733

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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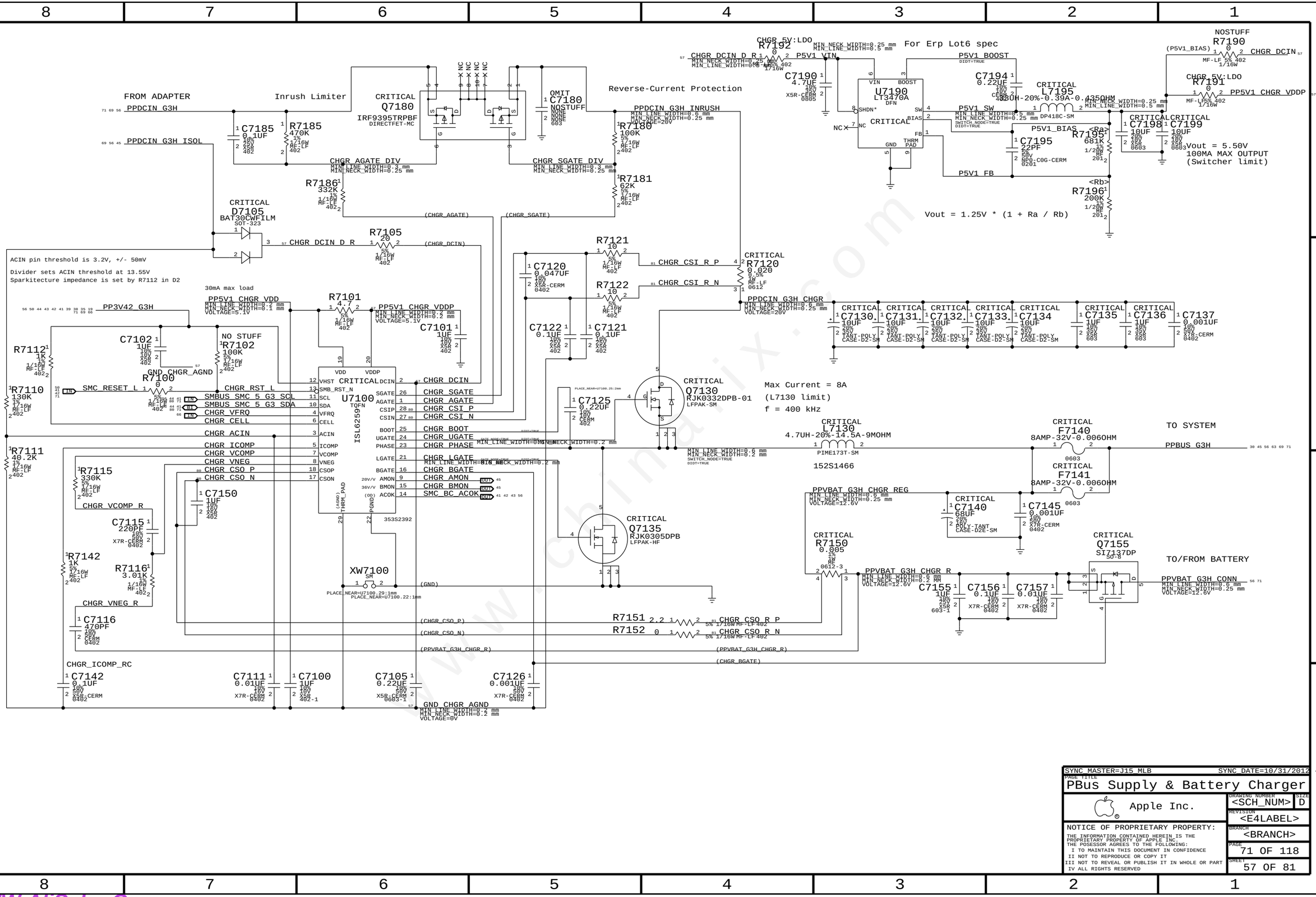

www.schimatix.com

SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE	PBus Supply & Battery Charger
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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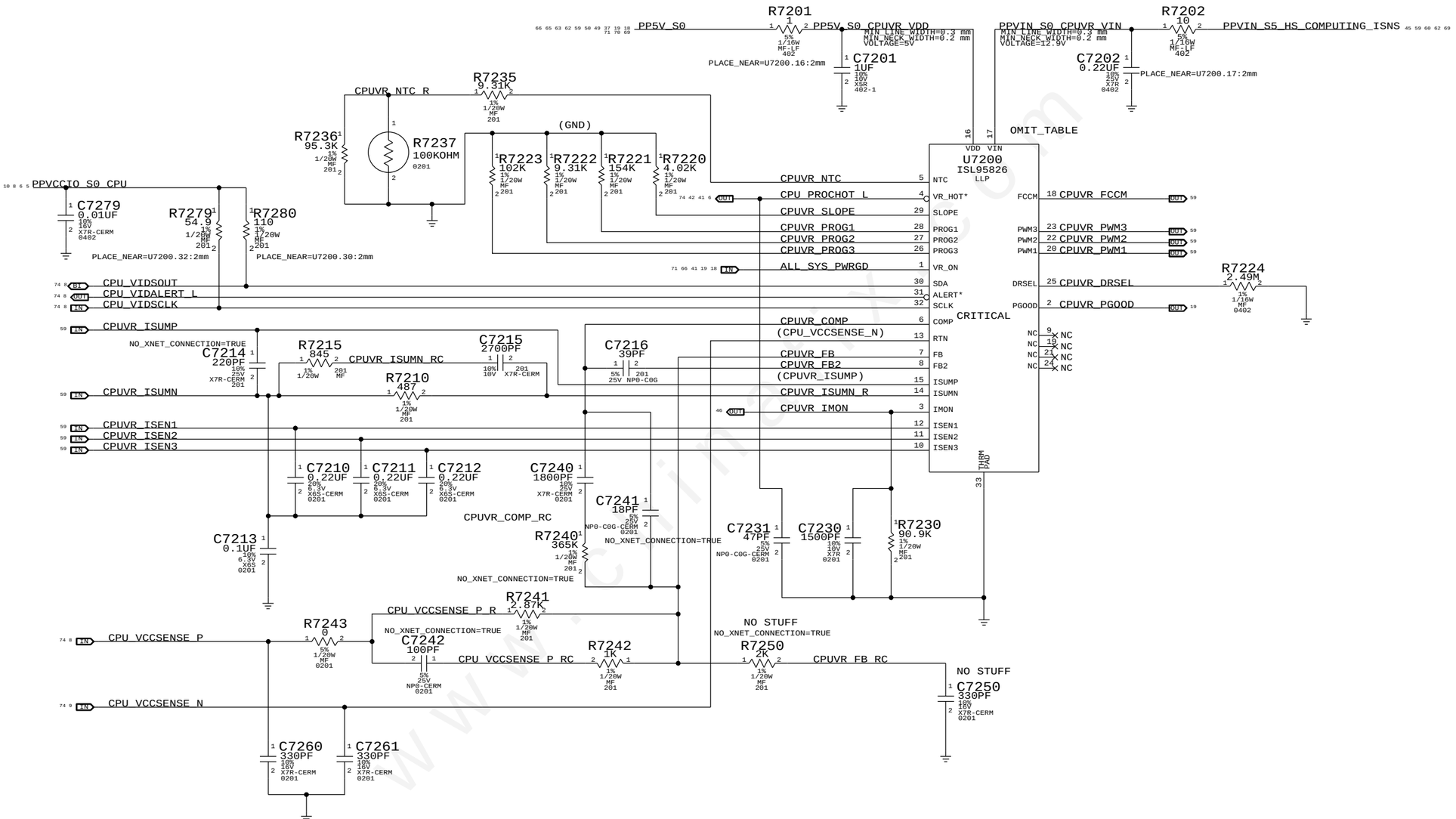
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826R6200,PWM,PGOOD,SCREEN,32P,QFN	U7200	CRITICAL	



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PAGE TITLE
CPU VR12.5 VCC Regulator IC

Apple Inc.

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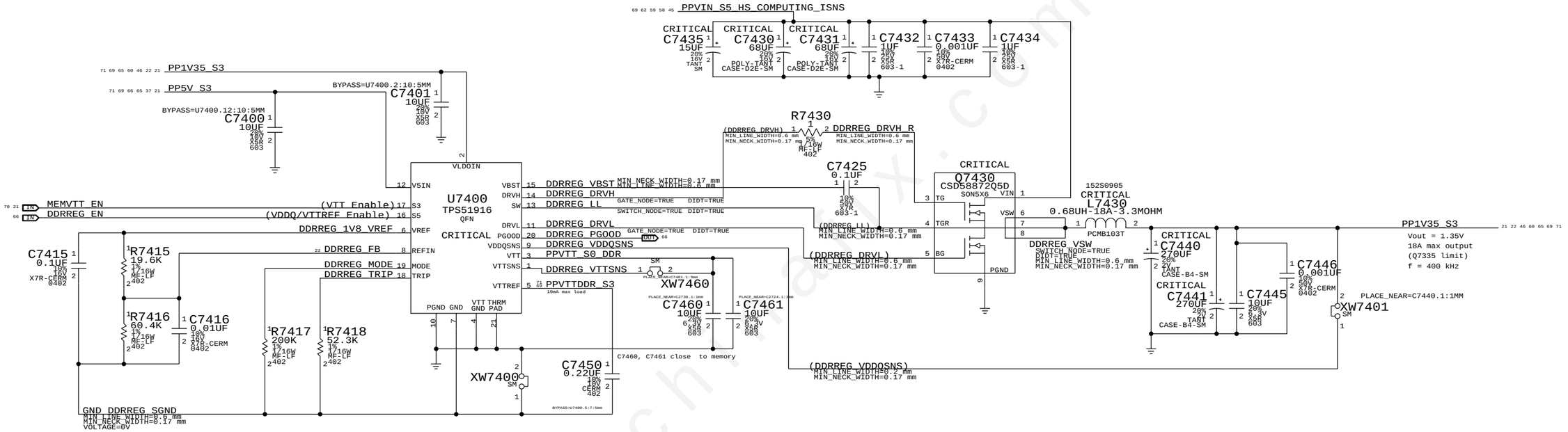
DDR3L (1V35 S3) REGULATOR



SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE	1.35V DDR3L SUPPLY
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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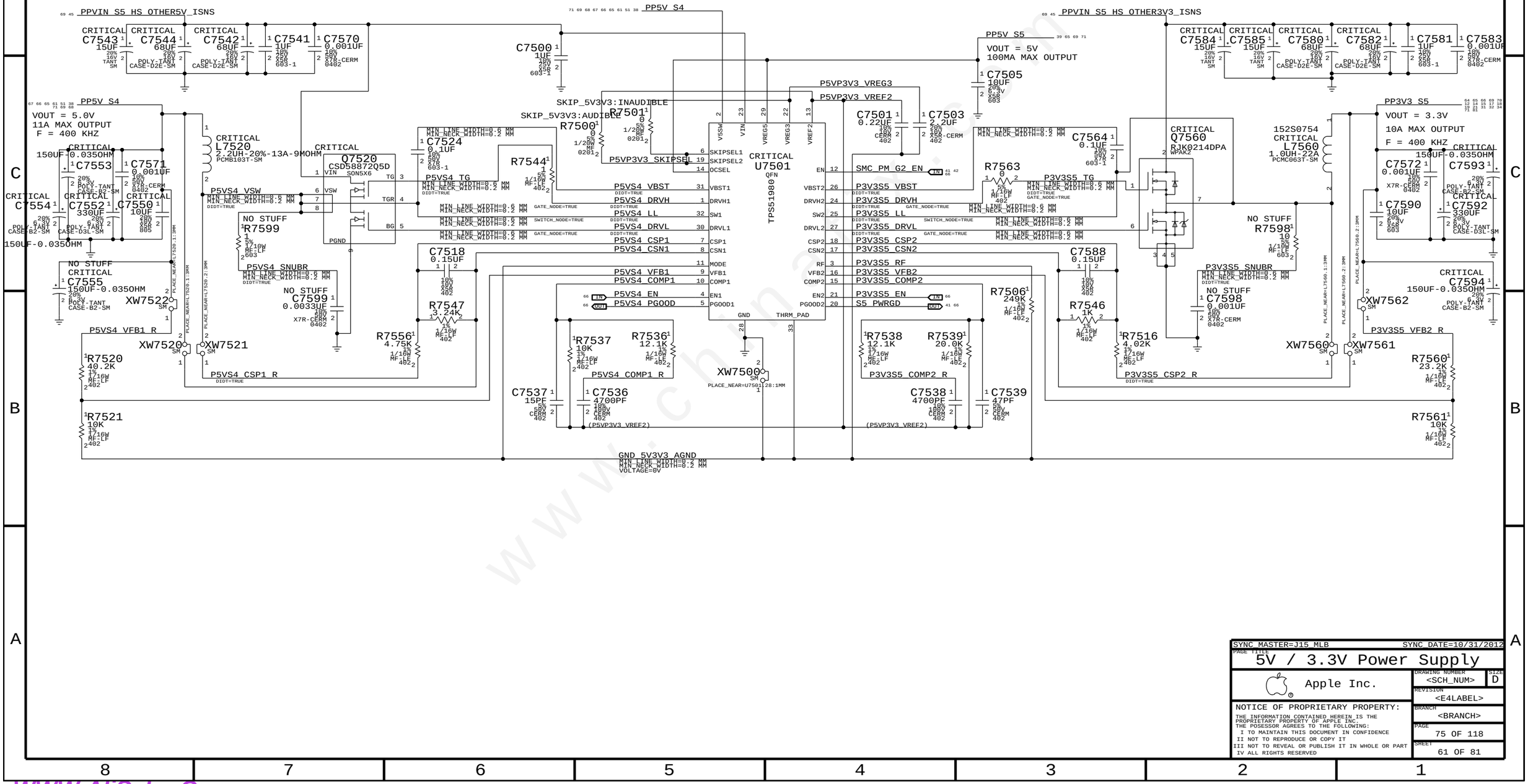

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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: 5V / 3.3V Power Supply

Apple Inc.

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1V05 S0 REGULATOR

PLACE_NEAR=U1100.AJ12:1MM
XW7601
SM
PP1V05_S0
P1V05S0_SENSE_P
PLACE_NEAR=U1100.AK14:1MM
XW7602
SM
P1V05S0_SENSE_N
Vout = 0.5V * (1 + Ra / Rb)
R7604 3.01K 1% 1/10W MF-LF 402
R7644 3.01K 1% 1/10W MF-LF 402 <Ra>
R7605 2.74K 1% 1/10W MF-LF 402 <Rb>
R7645 2.74K 1% 1/16W MF-LF 402 <Rb>
C7604 10PF 5% 50V C0G-CERM 0402
C7605 10PF 5% 50V C0G-CERM 0402
PPVIN_S5_HS_COMPUTING_ISNS
PP5V_S0
R7601 2.2 5% 1/10W MF-LF 402
C7601 10UF 20% 10V X5R 603
BYPASS=Q9800.14:16:5mm
P1V05S0_BOOT_RC MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm DIDT=TRUE
R7630 0 5% 1/10W MF-LF 603
C7630 1UF 10% 16V X5R 402
C7620 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7621 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7622 1000PF 5% 25V CERM 0402
BYPASS=Q7630.2:5:6mm
PP5V_S0_P1V05S0_VCC MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5V
U7600 ISL95870 UTQFN CRITICAL
VCC PVCC
EN FB SREF VO OCSET PGOOD RTN FSEL
BOOT UGATE PHASE LGATE
GND PGND
P1V05S0_VBST MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm DIDT=TRUE
P1V05S0_DRVH MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm GATE_NODE=TRUE DIDT=TRUE
P1V05S0_LL MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm SWITCH_NODE=TRUE DIDT=TRUE
P1V05S0_DRVL MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm GATE_NODE=TRUE DIDT=TRUE
P1V05S0_EN
P1V05S0_FB
P1V05S0_SREF
P1V05S0_VO
P1V05S0_OCSET
P1V05S0_PGOOD
P1V05S0_RTN
P1V05S0_FSEL
NO STUFF
R7603 0 5% 1/16W MF-LF 402
C7602 2.2UF 10% 16V X5R 603
C7603 0.047UF 10% 16V X7R-CERM 0402
P1V05S0_AGND MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V
XW7600 SM PLACE_NEAR=U7600.1:1mm
376S0953
CRITICAL
Q7630 RJK0214DPA WPAK2
L7630 CRITICAL 0.68UH-25A-5.5MOHM PCMC063T-SM 152S0955
R7640 CRITICAL 0.001 1% 1W MF-1 0612
PP1V05_S0_REG_R2 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.05V
PP1V05_S0
Vout = 1.05V
12A MAX OUTPUT
f = 300 kHz
C7623 1000PF 5% 25V CERM 0402 PLACE_NEAR=L7630.2:1.5mm
C7649 CRITICAL 270UF 20% 2V TANT CASE-B4-SM
C7648 CRITICAL 270UF 20% 2V TANT CASE-B4-SM
P1V05S0_CS_P
P1V05S0_CS_N
R7641 1.2K 5% 1/16W MF-LF 402
C7640 0.0018UF 10% 50V X7R-CERM 0402
R7642 1.2K 5% 1/16W MF-LF 402
(PCHVCCIOS0_OCSET)
(PCHVCCIOS0_VO)
OCP = R7641 x 8.5uA / R7640
OCP = 14.4A

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012
PAGE TITLE: 1V05V POWER SUPPLY
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Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7717,R7718,R7719,R7720,R7721,R7722,R7723,R7724		BKLT:PROD

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

C7715, C7716 SHOULD BE PLACED MIRRORED

C7718, C7719 SHOULD BE PLACED MIRRORED

C7720, C7721 SHOULD BE PLACED MIRRORED

C7723, C7724 SHOULD BE PLACED MIRRORED

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PAGE TITLE: LCD/KBD Backlight Driver

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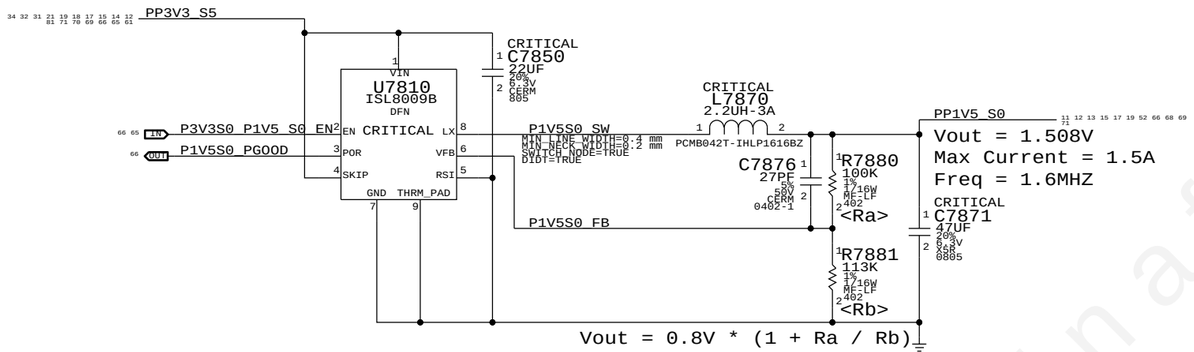
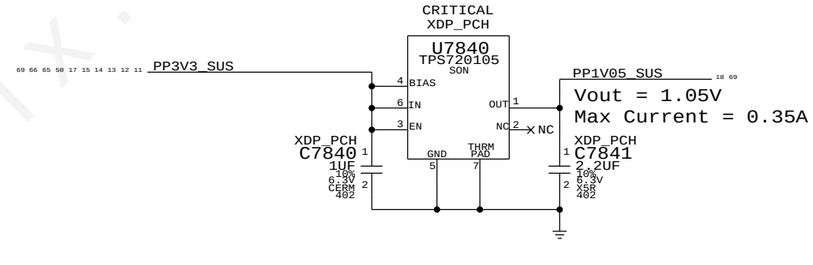
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



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PAGE TITLE: Misc Power Supplies

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3.3V S4 FET

376S0945
CRITICAL
Q8000
SIA413DJ
SC70-6L

EDP is per J45 Power Budget rev5

PP3V3_S5 → Q8002 DMN5L06VK-7 SOT-563 (D 6, G 2, S 1)
R8002 220K 5% 1/16W MF-LF 402
C8009 0.033UF 10% 16V X5R 402
R8000 47K 5% 1/16W MF-LF 402
C8000 0.01UF 10% 16V X7R-CERM 0402
P3V3S4_EN_L
P3V3S3_S4
PP3V3_S4
EN: S4_PWR_EN

3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

CRITICAL
Q8010
SIA413DJ
SC70-6L

PP3V3_S5 → Q8012 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 (D 3, G 1, S 2)
R8012 47K 5% 1/16W MF-LF 402
C8011 0.033UF 10% 16V X5R 402
R8010 39K 5% 1/16W MF-LF 402
C8010 0.01UF 10% 16V X7R-CERM 0402
P3V3S3_EN_L
P3V3S3_SS
PP3V3_S3
EN: P3V3S3_EN

3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

SSD_PWR_EN:GPIO
R8073 0 0201 1/20W 5% MF
SSD_PWR_EN
R8074 0 0201 1/20W 5% MF
PM_SLP_S3_BUF_L
SSD_PWR_FET_EN

5V S3 FET

CRITICAL
Q8050
SIA427DJ
SC70-6L

PP5V_S4 → Q8052 DMN5L06VK-7 SOT-563 (D 6, G 2, S 1)
R8052 200K 5% 1/16W MF-LF 402
C8051 0.033UF 10% 16V X5R 402
R8050 5.1K 5% 1/16W MF-LF 402
C8050 0.01UF 10% 16V X7R-CERM 0402
P5V3S3_EN_L
P5V3S3_SS
PP5V_S3
EN: P5V3S3_EN

5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

PP5V_S5
C8001 0.1UF 20% 10V CERM 402
U8001 SLG5AP1438V TDFN CRITICAL (VDD 1, CAP 7, ON 2, D 3, S 5, GND 8)
C8002 0.018UF 10% 16V X7R 402
P1V35CPU_SLEW_CTL
CPUVDDQ_EN
Slew rate : 0.8V/ms = 19.75nF
PP1V35_S3
PP1V35_S3RS0_FET

1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SENSOR_NONPROD_R
XW8005 SM
PP1V35_S3RS0_CPUDDR
NC_ISNS_CPUDDRN
NC_ISNS_CPUDDRP

3.3V SUS FET

CRITICAL
Q8020
SIA413DJ
SC70-6L

PP3V3_S5 → Q8002 DMN5L06VK-7 SOT-563 (D 3, G 5, S 4)
R8022 100K 5% 1/16W MF-LF 402
C8021 0.033UF 10% 16V X5R 402
R8020 12K 5% 1/16W MF-LF 402
C8020 0.01UF 10% 16V X7R-CERM 0402
P3V3SUS_EN_L
P3V3SUS_SS
PP3V3_SUS
EN: PM_SLP_SUS

3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

PLACE_NEAR=R5549.2:6mm
CRITICAL
Q8070
SI7615DN
PWRPK-1212-8

PP3V3_S5 → Q8072 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 (D 3, G 1, S 2)
R8072 47K 5% 1/16W MF-LF 402
C8071 0.033UF 10% 16V X5R 402
R8070 33K 5% 1/16W MF-LF 402
C8070 0.01UF 10% 16V X7R-CERM 0402
P3V3_SSD_EN_L
P3V3_SSD_SS
PP3V3_S0SW_SSD_R
SSD_PWR_FET_EN

3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

CRITICAL
Q8060
SI7615DN
PWRPK-1212-8

PP5V_S4
R8062 270K 5% 1/16W MF-LF 402
C8061 0.12UF 10% 10.0V X5R 402
R8060 6.2K 5% 1/16W MF-LF 402
C8060 0.47UF 10% 10V X5R 0402
P5V0S0_EN_L
P5V0S0_SS
PP5V_S0

Q8052 DMN5L06VK-7 SOT-563 (D 3, G 5, S 4)
EN: P5VS0_EN

5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 Switch

U8030
APN 353S2741

U8030	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

U8030 TPS22924 CSP (A2 VIN, B2 VIN, A1 VOUT, B1 VOUT, C2 ON, GND, C1 CRITICAL)
PP3V3_S5
P3V3S0_P1V5_S0_EN
PP3V3_S0
Max Current = 2A
C8030 1UF 10% 6.3V X5M 402

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012
PAGE TITLE: Power FETs
Apple Inc.
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Power State Debug LEDs
(For development only)

PP3V3_S5 → R8194 0 (PLACE_SIDE=BOTTOM, MIN_NECK_WIDTH=0.1 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=3.3V)

DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0	
R8190 20K 5% 1/20W MF 201	R8191 20K 5% 1/20W MF 201	R8192 20K 5% 1/20W MF 201	R8193 20K 5% 1/20W MF 201	
D8190	D8191	D8192	D8193	DBGLED
GREEN-56MCD-2MA-2.65V LTQH9G-SM	GREEN-56MCD-2MA-2.65V LTQH9G-SM	GREEN-56MCD-2MA-2.65V LTQH9G-SM	GREEN-56MCD-2MA-2.65V LTQH9G-SM	PLACE_SIDE=BOTTOM
PLACE_SIDE=BOTTOM SILK_PART=S5_ON	PLACE_SIDE=BOTTOM SILK_PART=S4_ON	PLACE_SIDE=BOTTOM SILK_PART=S3_ON	PLACE_SIDE=BOTTOM SILK_PART=S0_ON	
DBGLED_S4_D	DBGLED_S3_D	DBGLED_S0_D		
Q8190 DMN5L06VK-7 SOT-563	Q8190 DMN5L06VK-7 SOT-563	Q8191 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2		DBGLED

S4_PWR_EN, PM_SLP_S4_L, PM_SLP_S3_BUF_L

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S4 Power Enable

PP3V3_S5 → C8170 0.1uF → PM_SLP_S5_L:100K pull down on PCH page
PM_SLP_S5_L, SMC_S4_WAKESRC_EN → U8170 74LVC1G32 SOT891 → S4_PWR_EN (MAKE_BASE=TRUE)
S4_PWR_EN → R8174 43K, D8174 BAT54XV2T1, R8175 240, C8174 2.2UF
P5VS4_EN_D → P5VS4_EN
S4_PWR_EN → S4 PWR EN (x3)

S3 ENABLE

PM_SLP_S4_L → R8111 5.1K, R8112 0, R8113 0, R8114 3.3K
PM_SLP_S4_L:100K pull down in PCH page
C8110 0.47UF, C8112 0.47UF, C8113 0.47UF, C8114 0.47UF
TPAD_VBUS_EN
P5VS3_EN — P5VS3_EN (MAKE_BASE=TRUE)
P3V3S3_EN — P3V3S3_EN (MAKE_BASE=TRUE)
DDRREG_EN — DDRREG_EN (MAKE_BASE=TRUE)

CPUVCORE ENABLE

ALL_SYS_PWRGD — ALL_SYS_PWRGD (MAKE_BASE=TRUE)

3.3V SUS Enable

PM_SLP_SUS_L — PM_SLP_SUS_L (MAKE_BASE=TRUE)
PM_SLP_SUS_L: 100K pull down on PCH page

S0 ENABLE

PP3V3_S5 → C8180 0.1uF
MC74VHC1G08 SC70-HF (U8180)
(PM_SLP_S3_BUF_L) → NO STUFF R8180 100K, D8185 BAT54XV2T1
PM_SLP_S3_L → R8178 100 → PM_SLP_S3_R_L (MAKE_BASE=TRUE)
PM_SLP_S3_L:100K pull down in PCH page
R8185 130K, R8186 20K, R8187 0
P1V05_EN_D → R8138 820 → P1V05S0_EN (MAKE_BASE=TRUE)
C8185 0.82UF, C8186 0.68UF, C8187 0.68UF NO STUFF
P5VS0_EN — P5VS0_EN (MAKE_BASE=TRUE)
P3V3S0_P1V5_S0_EN — P3V3S0_P1V5_S0_EN (MAKE_BASE=TRUE)
P1V05S0_EN — P1V05S0_EN (MAKE_BASE=TRUE)
PM_SLP_S3_R_L, PM_SLP_S3_BUF_L

S0 Rail PGOOD (BJT Version)

PP5V_S0 → R8151 54.9K → VMON_5V_DIV (5.0V Divider:1.07V) → R8152 15.0K
PP3V3_S5 → R8156 150K → S0PGD_C
R8153 1K VMON_Q2_BASE, R8154 1K VMON_Q3_BASE, R8155 1K VMON_Q4_BASE
PP1V35_S3RS0_CPUDDR → R8154
PP3V3_S0 → R8158 15.0K → VMON_3V3_DIV (3V3 Divider:1.07V) → R8159 7.15K
Q8150 ASMCC0179 DFN2015H4-8 353S2809 (Q1 Q2 Q3 Q4 CRITICAL)
Vbe 0.7V max @2mA
Vce(sat) 0.1V max @1mA
Q1 Vth 0.7~1V @Id 250uA
S0PGD_BJT_GND_R → R8157 100
ALL_SYS_PWRGD → S0PGD_C

3.3V SUS Detect

PP3V3_S5 → C8130 0.1uF
No stuff C8131, 12ms Min delay time
U8130 Sense input threhold is 3.07V
U8130 TPS3808G33DBVRG4 SOT23-6 (SENSE, RESET*, CT, MR*, VDD, GND) CRITICAL
C8131 0.001UF NO STUFF
PP3V3_SUS → R8133 100K → PM_RSMRST_L (PM_RSMRST_L goes to U1100.C21)
SUS_PGOOD_CT
TP_SUS_PGOOD_MR_L

S5 Rail Enables & PGOOD

PP3V42_G3H → R8141 100K
S5_PWRGD-->SMC
SMC-->PM_DSW_PWRGD
S5_PWRGD — S5_PWRGD (MAKE_BASE=TRUE)
SMC_PM_G2_EN → R8140 100 → SMC_PM_G2_EN (MAKE_BASE=TRUE)
P3V3S5_EN — P3V3S5_EN (MAKE_BASE=TRUE)
NO STUFF C8142 0.0033UF

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.

PP3V3_S4 → R8125 330K → PM_WLAN_EN (MAKE_BASE=TRUE)

S0 Rail PGOOD Circuitry
(ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 0.815V-3.009V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V
keep R8171 DDRCPU 1.35V only

PP3V3_S0 → C8162 0.1UF, C8160 0.1UF
PP3V3_S0_VMON_P2 → R8195 10
PP3V3_S0_VMON_P7 → R8196 10, NOSTUFF R8197 100K
C8161 0.1UF, C8163 0.1UF
PP1V35_S3RS0_CPUDDR
PP1V05_S0
R8160 6.04K, R8170 10K, R8172 6.04K
R8161 15.0K, R8171 12.4K, R8173 15.0K
1V35_VMON divider 0.716V @1.31V
1V05_VMON divider 0.716V @1.02V
U8160 ISL88042IRTEZ TDFN (V2MON 353S2310 CRITICAL, V3MON, V4MON, VDD, GND, THRM_PAD, RST*, 1VMON_MR)
S0PGOOD_ISL
P1V5S0_PGOOD from U7810
P1V5S0_PGOOD → R8167 10K, R8168 100
P1V05S0_PGOOD → R8169 100
PM_SLP_S3_BUF_L
ALL_SYS_PWRGD_R → R8162 330 → ALL_SYS_PWRGD

1V5 S0 "PGOOD" Delay

PP3V3_S5 → R8136 23.7K, C8134 2.2UF
PM_1V5_PGD_L → R8139 2.0K
CRITICAL Q8151 DMB53D0UV SOT-563 (Vgs:0.7V~1.0V)
PM_1V5_PGD_L_R → R8135 54.9K, R8134 61.9K
PM_1V5_PGD_DIV
VBEon: 0.58~0.7V
1V5 Divider:0.75~0.85V
DELAY_1V5S0_PGD → R8137 100 → ALL_SYS_PWRGD

CHGR VFRQ Generation

VFRQ High: Variable Frequency
VFRQ Low: Fix Frequency
PP3V42_G3H → R8131 100K → CHGR_VFRQ

Unused PGOOD signals

Q8131 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
DDRREG_PGOOD
P5VS4_PGOOD
PP5V_S3 → R8120 470K → PP5V_S4 → R8165 470K

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LCD PANEL INTERFACE (eDP)

LCD Panel HPD & AUX strapping

C8350 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8351 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8352 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8353 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8354 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8355 9.1PF ±/-0.1PF C0G-CERM 0201 50V

71 63 LED_RETURN_6
71 63 LED_RETURN_5
71 63 LED_RETURN_4
71 63 LED_RETURN_3
71 63 LED_RETURN_2
71 63 LED_RETURN_1

71 63 PPVOUT_S0_LCDBKLT

CRITICAL
J8300
20525-130E-01
F-RT-SM

NC

518S0829

20 OUT LCD_HPD
R8300 0 5% 1/20W MF 0201
73 67 LCD_HPD_CONN
71 63 OUT LCD_FSS

74 70 5 IN DP_INT_AUXCH_C_P C8328 0.1UF 10% 16V XSR-CERM 0201
74 70 5 IN DP_INT_AUXCH_C_N C8329 0.1UF 10% 16V XSR-CERM 0201
74 71 67 DP_INT_AUX_P
74 71 67 DP_INT_AUX_N

74 70 5 IN DP_INT_ML_C_P<0> C8320 0.1UF
74 70 5 IN DP_INT_ML_C_N<0> C8321 0.1UF
74 70 5 IN DP_INT_ML_C_P<1> C8322 0.1UF
74 70 5 IN DP_INT_ML_C_N<1> C8323 0.1UF
74 70 5 IN DP_INT_ML_C_P<2> C8324 0.1UF
74 70 5 IN DP_INT_ML_C_N<2> C8325 0.1UF
74 70 5 IN DP_INT_ML_C_P<3> C8326 0.1UF
74 70 5 IN DP_INT_ML_C_N<3> C8327 0.1UF
(10% XSR-CERM 16V 0201)

74 DP_INT_ML_F_P<0> 150OHM-100MA-8.5GHZ DLP0NS SYM_VER-1 CRITICAL FL8300 74 71 67 DP_INT_ML_P<0>
74 DP_INT_ML_F_N<0> CRITICAL FL8300 74 71 67 DP_INT_ML_N<0>
74 DP_INT_ML_F_P<1> 150OHM-100MA-8.5GHZ DLP0NS SYM_VER-1 CRITICAL FL8301 74 71 67 DP_INT_ML_P<1>
74 DP_INT_ML_F_N<1> CRITICAL FL8301 74 71 67 DP_INT_ML_N<1>
74 DP_INT_ML_F_P<2> 150OHM-100MA-8.5GHZ DLP0NS SYM_VER-2 CRITICAL FL8302 74 71 67 DP_INT_ML_P<2>
74 DP_INT_ML_F_N<2> CRITICAL FL8302 74 71 67 DP_INT_ML_N<2>
74 DP_INT_ML_F_P<3> 150OHM-100MA-8.5GHZ DLP0NS SYM_VER-1 CRITICAL FL8303 74 71 67 DP_INT_ML_P<3>
74 DP_INT_ML_F_N<3> CRITICAL FL8303 74 71 67 DP_INT_ML_N<3>

71 70 12 IN EDP_IG_PANEL_PWR

CRITICAL
U8300
FPF1009
MFET-2X2-BIN

1 ON
2 VIN_1
3 VIN_2
4 VOUT_1
5 VOUT_2
6 GND
7 THRM PAD

71 69 68 66 65 61 51 38 PP5V_S4

C8309 0.1UF 10% 16V X7R-CERM 0402
C8311 0.1UF 10% 16V X7R-CERM 0402
C8312 10UF 20% 6.3V X5R 603

PP5VR3V3_SW_LCD_ISNS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

SENSOR_NONPROD_R
XW8320
SM

NC_ISNS_LCD_PANELN OUT
NC_ISNS_LCD_PANELP OUT

PP5VR3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CRITICAL
L8300
FERR-220-OHM
0805

C8301 0.1UF 10% 16V X7R-CERM 0402
C8302 0.001UF 10% 50V X7R-CERM 0402

71 PP5VR3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C8300 1000PF 10% 100V X7R 0603

33 29 20 10 81 71 69 66 65 55 63 61 49 12 11 10 15 14 13 46 45 44 35 PP3V3_S0

R8303 1M 5% 1/20W MF 201
74 71 67 DP_INT_AUX_N
71 67 LCD_HPD_CONN
74 71 67 DP_INT_AUX_P
R8301 1M 5% 1/20W MF 201
R8302 1M 5% 1/20W MF 201

R8311 1M 5% 1/20W MF 201 — 74 71 67 DP_INT_ML_P<0>
R8312 1M 5% 1/20W MF 201 — 74 71 67 DP_INT_ML_N<0>
R8313 1M 5% 1/20W MF 201 — 74 71 67 DP_INT_ML_P<1>
R8314 1M 5% 1/20W MF 201 — 74 71 67 DP_INT_ML_N<1>
R8315 1M 5% 1/20W MF 201 — 74 71 67 DP_INT_ML_P<2>
R8316 1M 5% 1/20W MF 201 — 74 71 67 DP_INT_ML_N<2>
R8317 1M 5% 1/20W MF 201 — 74 71 67 DP_INT_ML_P<3>
R8318 1M 5% 1/20W MF 201 — 74 71 67 DP_INT_ML_N<3>

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eDP Display Connector

Apple Inc.

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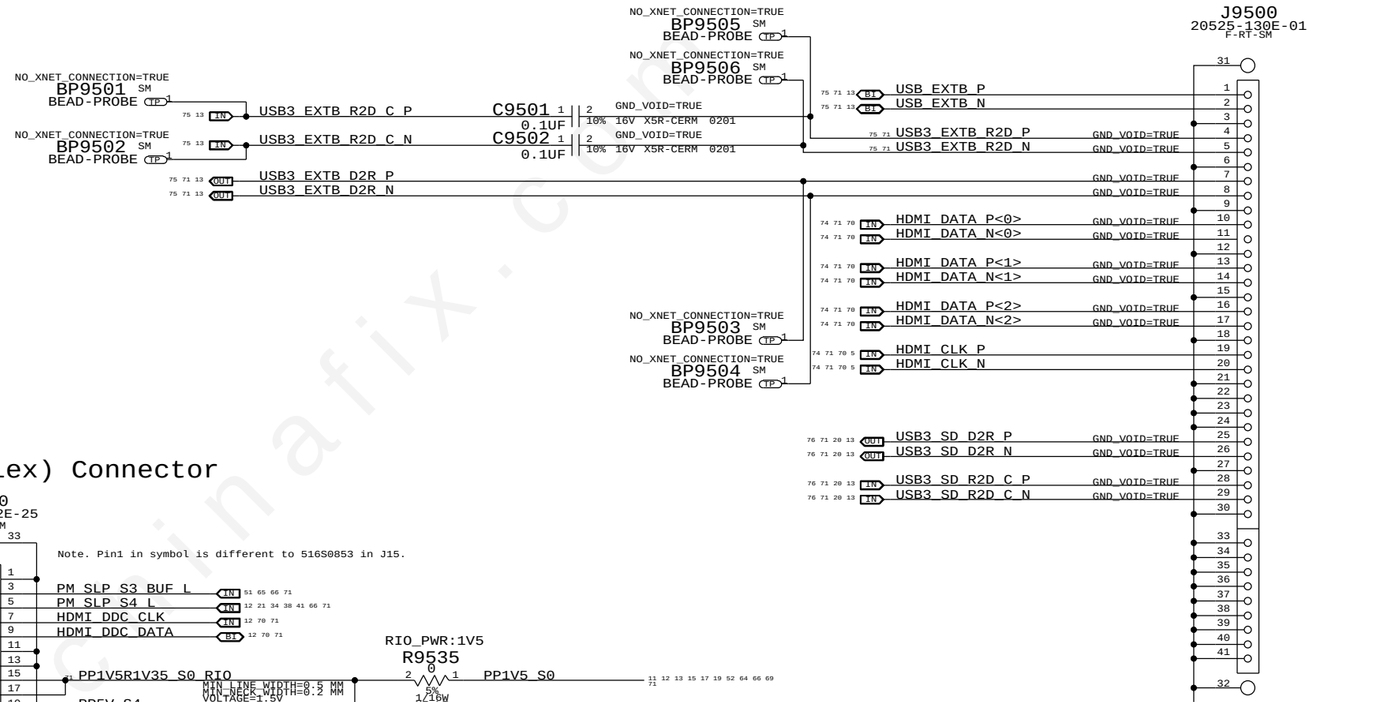
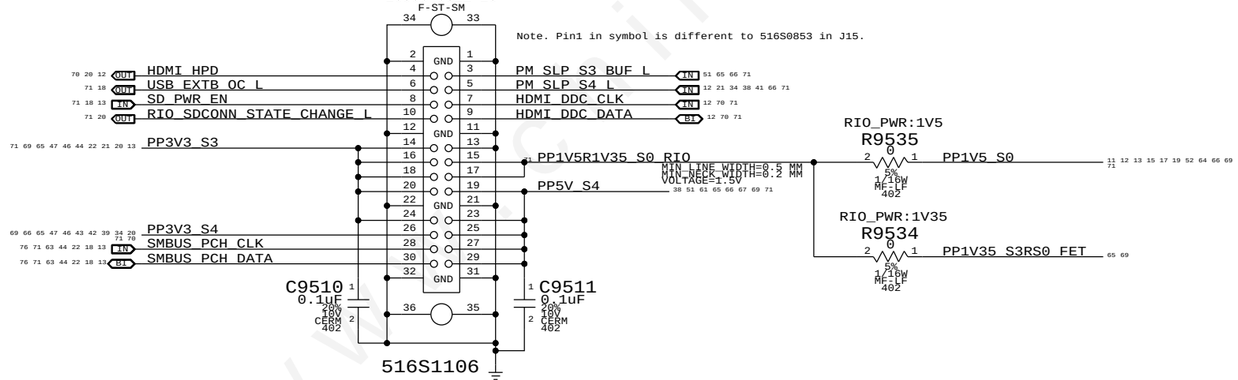
Wire-to-Board (Micro-coax) Connector



Board-to-Board (Flex) Connector



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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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Apple Inc.

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G3H/5V Rails

PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H

PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS

PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS

PPVIN_S5_HS_OTHER5V_ISNS
PPVIN_S5_HS_OTHER5V_ISNS
PPVIN_S5_HS_OTHER5V_ISNS

PPVIN_S4_TPAD
PPVIN_S4_TPAD
PPVIN_S4_TPAD

PPDCIN_G3H
PPDCIN_G3H
PPDCIN_G3H

PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL

PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H

PPVRTC_G3H
PPVRTC_G3H
PPVRTC_G3H

PP5V_S5
PP5V_S5
PP5V_S5

PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4

PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3

PP5V_S0
PP5V_S0
PP5V_S0

Display Aliases

71 70 67 12	EDP_IG_PANEL_PWR	MAKE_BASE=TRUE	=	EDP_IG_PANEL_PWR	12 67 70 71
71 70 63 12	EDP_IG_BKL_ON	MAKE_BASE=TRUE	=	EDP_IG_BKL_ON	12 63 70 71
70 63 12	EDP_IG_BKL_PWM	MAKE_BASE=TRUE	=	EDP_IG_BKL_PWM	12 63 70
74 67 5	DP_INT_ML_C_P<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_A_MLP<3..0>	
74 67 5	DP_INT_ML_C_N<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_A_MLN<3..0>	
74 70 67 5	DP_INT_AUXCH_C_P	MAKE_BASE=TRUE	=	DP_INT_AUXCH_C_P	5 67 70 74
74 70 67 5	DP_INT_AUXCH_C_N	MAKE_BASE=TRUE	=	DP_INT_AUXCH_C_N	5 67 70 74
70 28 12	DP_TBTSNK0_HPD	MAKE_BASE=TRUE	=	DP_TBTSNK0_HPD	12 28 70
74 28 5	DP_TBTSNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_B_MLP<3..0>	
74 28 5	DP_TBTSNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_B_MLN<3..0>	
74 70 28 12	DP_TBTSNK0_AUXCH_C_P	MAKE_BASE=TRUE	=	DP_TBTSNK0_AUXCH_C_P	12 28 70 74
74 70 28 12	DP_TBTSNK0_AUXCH_C_N	MAKE_BASE=TRUE	=	DP_TBTSNK0_AUXCH_C_N	12 28 70 74
70 33 12	DP_TBTSNK0_DDC_DATA	MAKE_BASE=TRUE	=	DP_TBTSNK0_DDC_DATA	12 33 70
70 33 12	DP_TBTSNK0_DDC_CLK	MAKE_BASE=TRUE	=	DP_TBTSNK0_DDC_CLK	12 33 70
70 28 12	DP_TBTSNK1_HPD	MAKE_BASE=TRUE	=	DP_TBTSNK1_HPD	12 28 70
74 28 5	DP_TBTSNK1_ML_C_P<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_C_MLP<3..0>	
74 28 5	DP_TBTSNK1_ML_C_N<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_C_MLN<3..0>	
74 70 28 12	DP_TBTSNK1_AUXCH_C_P	MAKE_BASE=TRUE	=	DP_TBTSNK1_AUXCH_C_P	12 28 70 74
74 70 28 12	DP_TBTSNK1_AUXCH_C_N	MAKE_BASE=TRUE	=	DP_TBTSNK1_AUXCH_C_N	12 28 70 74
70 33 12	DP_TBTSNK1_DDC_DATA	MAKE_BASE=TRUE	=	DP_TBTSNK1_DDC_DATA	12 33 70
70 33 12	DP_TBTSNK1_DDC_CLK	MAKE_BASE=TRUE	=	DP_TBTSNK1_DDC_CLK	12 33 70
70 68 20 12	HDMI_HPD	MAKE_BASE=TRUE	=	HDMI_HPD	12 20 68 70
74 71 68	HDMI_DATA_P<0..2>	MAKE_BASE=TRUE	=	TP_DP_IG_D_MLP<2..0>	5
74 71 68	HDMI_DATA_N<0..2>	MAKE_BASE=TRUE	=	TP_DP_IG_D_MLN<2..0>	5
74 71 70 68 5	HDMI_CLK_P	MAKE_BASE=TRUE	=	HDMI_CLK_P	5 68 70 71 74
74 71 70 68 5	HDMI_CLK_N	MAKE_BASE=TRUE	=	HDMI_CLK_N	5 68 70 71 74
71 70 68 12	HDMI_DDC_CLK	MAKE_BASE=TRUE	=	HDMI_DDC_CLK	12 68 70 71
71 70 68 12	HDMI_DDC_DATA	MAKE_BASE=TRUE	=	HDMI_DDC_DATA	12 68 70 71

CPU signals

70 60 21	MEMVTT_EN	MAKE_BASE=TRUE	=	MEMVTT_EN	21 60 70

Thunderbolt Signals Through PEG

74 28 5	PCIE_TBT_D2R_P<3..0>	MAKE_BASE=TRUE	=	=PEG_D2R_P<3..0>	OUT
74 28 5	PCIE_TBT_D2R_N<3..0>	MAKE_BASE=TRUE	=	=PEG_D2R_N<3..0>	OUT
74 28 5	PCIE_TBT_R2D_C_P<3..0>	MAKE_BASE=TRUE	=	=PEG_R2D_C_P<3..0>	IN
74 28 5	PCIE_TBT_R2D_C_N<3..0>	MAKE_BASE=TRUE	=	=PEG_R2D_C_N<3..0>	IN

Unused PEG Lanes

5	TP_PEG_D2RP<15..4>	MAKE_BASE=TRUE	=	=PEG_D2R_P<15..4>	
5	TP_PEG_D2RN<15..4>	MAKE_BASE=TRUE	=	=PEG_D2R_N<15..4>	
5	TP_PEG_R2D_CP<15..4>	MAKE_BASE=TRUE	=	=PEG_R2D_C_P<15..4>	
5	TP_PEG_R2D_CN<15..4>	MAKE_BASE=TRUE	=	=PEG_R2D_C_N<15..4>	

70 49 PP3V3_S3_FAN_CTL

RA201
0
1 2
5%
1/20W
MF
0201

RA202
NOSTUFF

PP3V3_S3_FAN_CTL
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
49 70

PP3V3_S5
12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 71 81

PP3V3_S4
20 34 39 42 43 46 47 65 66 68 69 71

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
14	DPMUX_UC_IRQ
11	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L

		VOLTAGE	MAKE_BASE		
77 74 70 24 23 22	PP0V75_S3_MEM_VREFDQ_A	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 74 77
74 70 26 25 22	PP0V75_S3_MEM_VREFDQ_B	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70 74
77 74 70 24 23 22	PP0V75_S3_MEM_VREFCA_A	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 74 77
74 70 26 25 22	PP0V75_S3_MEM_VREFCA_B	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_B	22 25 26 70 74

65 63 62 59 58 50 49 37 19 18 71 69 66 PP5V_S0

XWA202
SM
1 2
PP5V_S0_AUDIO_AMP_L
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
53

XWA203
SM
1 2
PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
53

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Signal Aliases

Apple Inc.

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Functional Test Points

J3501 - airport

FUNC_TEST		
TRUE	AP_CLKREQ_Q_L	34
TRUE	AP_RESET_CONN_L	34
TRUE	PCIE_AP_D2R_PI_N	34 76
TRUE	PCIE_AP_D2R_PI_P	34 76
TRUE	PCIE_AP_R2D_N	34 76
TRUE	PCIE_AP_R2D_P	34 76
TRUE	PCIE_CLK100M_AP_CONN_N	34 76
TRUE	PCIE_CLK100M_AP_CONN_P	34 76
TRUE	PCIE_WAKE_L	12 34 36 76
TRUE	PP3V3_S3RS4_BT_F	34
TRUE	PP3V3_WLAN	34 42
TRUE	USB_BT_CONN_N	34 75
TRUE	USB_BT_CONN_P	34 75
TRUE	WIFI_EVENT_L	34 41 42
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	37 79
TRUE	MIPI_CLK_CONN_P	37 79
TRUE	CAM_SENSOR_WAKE_L_CONN	37
TRUE	MIPI_DATA_CONN_N	37 79
TRUE	MIPI_DATA_CONN_P	37 79
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 80
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 80
TRUE	I2C_CAM_SCK	36 37
TRUE	I2C_CAM_SDA	36 37
TRUE	PP5V_S3RS0_ALSCAM_F	37
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	5 68 70 74
TRUE	HDMI_CLK_P	5 68 70 74
TRUE	HDMI_DATA_N<0>	68 70 74
TRUE	HDMI_DATA_N<1>	68 70 74
TRUE	HDMI_DATA_N<2>	68 70 74
TRUE	HDMI_DATA_P<0>	68 70 74
TRUE	HDMI_DATA_P<1>	68 70 74
TRUE	HDMI_DATA_P<2>	68 70 74

TRUE	USB3_SD_D2R_N	13 20 68 76
TRUE	USB3_SD_D2R_P	13 20 68 76
TRUE	USB3_SD_R2D_C_N	13 20 68 76
TRUE	USB3_SD_R2D_C_P	13 20 68 76
TRUE	USB3_EXTB_D2R_N	13 68 75
TRUE	USB3_EXTB_D2R_P	13 68 75
TRUE	USB3_EXTB_R2D_N	68 75
TRUE	USB3_EXTB_R2D_P	68 75
TRUE	USB_EXTB_N	13 68 75
TRUE	USB_EXTB_P	13 68 75
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 68
TRUE	PP1V5R1V35_S0_RIO	68
TRUE	HDMI_DDC_CLK	12 68 70
TRUE	HDMI_DDC_DATA	12 68 70
TRUE	HDMI_HPD_L	
TRUE	SMBUS_PCH_CLK	13 18 22 44 63 68 76
TRUE	SMBUS_PCH_DATA	13 18 22 44 63 68 76
TRUE	PM_SLP_S3_BUF_L	51 65 66 68
TRUE	PM_SLP_S4_L	12 21 34 38 41 66 68
TRUE	PP3V3_S3	3X 13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S4	5X 38 51 61 65 66 67 68 69
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 68
TRUE	USB_EXTB_OC_L	18 68
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	SMC_LID_R	43
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6100 - lpc + spi

FUNC_TEST		
TRUE	LPCPLUS_GPIO	14 50
TRUE	LPCPLUS_RESET_L	20 50 76
TRUE	LPC_AD<0>	13 41 50 76
TRUE	LPC_AD<1>	13 41 50 76
TRUE	LPC_AD<2>	13 41 50 76
TRUE	LPC_AD<3>	13 41 50 76
TRUE	LPC_CLK33M_LPCPLUS	19 50 76
TRUE	LPC_FRAME_L	13 41 50 76
TRUE	LPC_PWRDWN_L	12 20 41 50
TRUE	LPC_SERIRQ	13 41 50
TRUE	PM_CLKRUN_L	12 41 50
TRUE	PP5V_S0	18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	SMC_RESET_L	41 42 50 57
TRUE	SMC_ROMBOOT	42 50
TRUE	SMC_RX_L	41 42 50
TRUE	SMC_TCK	41 42 50
TRUE	SMC_TDI	41 42 50
TRUE	SMC_TDO	41 42 50
TRUE	SMC_TMS	41 42 50
TRUE	SMC_TX_L	41 42 50
TRUE	SPIROM_USE_MLB	14 50
TRUE	SPI_ALT_CLK	50
TRUE	SPI_ALT_CS_L	50
TRUE	SPI_ALT_MISO	50
TRUE	SPI_ALT_MOSI	50
TRUE	TP_SMC_MD1	50
TRUE	TP_SMC_TRST_L	50
TRUE	GND	2X

J4800 - ipd flex

TRUE	Z2_CS_L	39
TRUE	Z2_MOSI	39
TRUE	Z2_MISO	39
TRUE	Z2_SCLK	39
TRUE	Z2_HOST_INTN	39
TRUE	Z2_CLKIN	39
TRUE	Z2_KEY_ACT_L	39
TRUE	PSOC_F_CS_L	39
TRUE	PICKB_L	39
TRUE	PSOC_MOSI	39
TRUE	PSOC_MISO	39
TRUE	PSOC_SCLK	39
TRUE	SMBUS_SMC_2_S3_SCL	39 41 44 80
TRUE	SMBUS_SMC_2_S3_SDA	39 41 44 80
TRUE	SMC_LID	39 41 42 43
TRUE	SMC_T101_COM_1	
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S5	39 61 65 69 71
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	WS_CONTROL_KBD	39
TRUE	WS_KBD1	39
TRUE	WS_KBD10	39
TRUE	WS_KBD11	39
TRUE	WS_KBD12	39
TRUE	WS_KBD13	39
TRUE	WS_KBD14	39
TRUE	WS_KBD15_CAP	39
TRUE	WS_KBD16_NUM	39
TRUE	WS_KBD17	39
TRUE	WS_KBD18	39
TRUE	WS_KBD19	39
TRUE	WS_KBD2	39
TRUE	WS_KBD20	39
TRUE	WS_KBD21	39
TRUE	WS_KBD22	39
TRUE	WS_KBD23	39
TRUE	WS_KBD3	39
TRUE	WS_KBD4	39
TRUE	WS_KBD5	39
TRUE	WS_KBD6	39
TRUE	WS_KBD7	39
TRUE	WS_KBD8	39
TRUE	WS_KBD9	39
TRUE	WS_KBD_ONOFF_L	39
TRUE	WS_LEFT_OPTION_KBD	39
TRUE	WS_LEFT_SHIFT_KBD	39
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 40 63
TRUE	KBDBKLT_RETURN2	2X 40 63
TRUE	PPVOUT_S0_KBDBKLT	40 63
TRUE	GND	4X

J6701 - audio flex

FUNC_TEST		
TRUE	AUD_HP_PORT_L	51 55
TRUE	AUD_HP_PORT_R	51 55
TRUE	AUD_SPDIF_OUT_JACK	
TRUE	AUD_TIPDET_INV	
TRUE	AUD_TYPEDET	51 55
TRUE	AUD_CONN_MIC_XW	4X
TRUE	CH_HS_MIC	
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	AUD_CONN_SLEEVE_XW	4X 54 55
TRUE	US_HS_MIC	
TRUE	GND	2X GND

J6601 - mic

TRUE	DMIC_CLK3	52 55
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	DMIC_SDA2	55
TRUE	DMIC_SDA3	52 55
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	52 55
TRUE	SPKRCONN_L_OUT_N	53 55 81
TRUE	SPKRCONN_L_OUT_P	53 55 81
TRUE	SPKRCONN_SL_OUT_N	53 55 81
TRUE	SPKRCONN_SL_OUT_P	53 55 81
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	52 55
TRUE	SPKRCONN_R_OUT_N	53 55 81
TRUE	SPKRCONN_R_OUT_P	53 55 81
TRUE	SPKRCONN_SR_OUT_N	53 55 81
TRUE	SPKRCONN_SR_OUT_P	53 55 81
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	41 44 56 57 80
TRUE	SMBUS_SMC_5_G3_SDA	41 44 56 57 80
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	67 74
TRUE	DP_INT_AUX_P	67 74
TRUE	DP_INT_ML_N<0>	67 74
TRUE	DP_INT_ML_N<1>	67 74
TRUE	DP_INT_ML_N<2>	67 74
TRUE	DP_INT_ML_N<3>	67 74
TRUE	DP_INT_ML_P<0>	67 74
TRUE	DP_INT_ML_P<1>	67 74
TRUE	DP_INT_ML_P<2>	67 74
TRUE	DP_INT_ML_P<3>	67 74
TRUE	LCD_FSS	63 67
TRUE	LCD_HPD_CONN	67
TRUE	LED_RETURN_1	63 67
TRUE	LED_RETURN_2	63 67
TRUE	LED_RETURN_3	63 67
TRUE	LED_RETURN_4	63 67
TRUE	LED_RETURN_5	63 67
TRUE	LED_RETURN_6	63 67
TRUE	PP5VR3V3_SW_LCD	3X 67
TRUE	PPVOUT_S0_LCDBKLT	63 67
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 41 66
TRUE	PPVTT_S0_DDR	21 27 60 69
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	PP3V3_S3	13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 81
TRUE	PP3V3_S5_AVREF_SMC	41 42
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	PP5V_S0	18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	PP5V_S3	21 37 60 65 66 69
TRUE	PP5V_S5	39 61 65 69 71
TRUE	PPBUS_G3H	30 45 56 57 63 69
TRUE	PPDCIN_G3H	56 57 69
TRUE	PPVCC_S0_CPU	6 8 10 46 59 69
TRUE	PPVTTDDR_S3	60 69
TRUE	PP3V3_S0SW_SSD	35 46 69
TRUE	PP1V5_S0	11 12 13 15 17 19 52 64 66 68 69
TRUE	PP1V35_S3	21 22 46 60 65 69

XDP

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 18 74
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 74
TRUE	XDP_CPU_TDO	6 18 74
TRUE	XDP_CPUPCH_TRST_L	6 18 74
TRUE	XDP_CPU_TMS	6 18 74
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 74
TRUE	XDP_CPU_PRDY_L	6 18 74
TRUE	PM_RSMRST_L	12 66 76
TRUE	PM_PCH_PWROK	12 19 76
TRUE	PM_SYSRST_L	12 19 41 76
TRUE	CPU_CFG<3>	6 18 74
TRUE	PP1V05_S0	14 15 17 18 42 62 66 69
TRUE	GND	2X GND

Power Sequence

FUNC_TEST		
TRUE	SMC_ONOFF_L	39 41 42
TRUE	PM_DSW_PWRGD	12 41 76
TRUE	ALL_SYS_PWRGD	18 19 41 58 66
TRUE	PM_PCH_SYS_PWROK	12 18 19 41 76
TRUE	PLT_RESET_L	12 18 20 21
TRUE	EDP_IG_PANEL_PWR	12 67 70
TRUE	EDP_IG_BKL_ON	12 63 70

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NC NO_TESTs

PCH

	NO_TEST	MAKE_BASE	
NC_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN	TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP	TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN	TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP	TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP	TRUE	TRUE	NC_USB3_EXTD_R2D_CP
NC_PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
NC_SATA_A_D2RN	TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP	TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN	TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP	TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN	TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP	TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN	TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP	TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP
NC_USB_EXTCN	TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP	TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN	TRUE	TRUE	NC_USB_SDN
NC_USB_SDP	TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
NC_USB_6N	TRUE	TRUE	NC_USB_6N
NC_USB_6P	TRUE	TRUE	NC_USB_6P
NC_USB_7N	TRUE	TRUE	NC_USB_7N
NC_USB_7P	TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN	TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP	TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN	TRUE	TRUE	NC_USB_IRN
NC_USB_IRP	TRUE	TRUE	NC_USB_IRP
NC_ITPXDP_CLK100MN	TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP	TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L
NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN
NC_SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

	NO_TEST	MAKE_BASE	
NC_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT
TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
NC_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP
NC_PCIE_CLK100M_GPUN	TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP	TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
NC_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
NC_USB_4N	TRUE	TRUE	NC_USB_4N
NC_USB_4P	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>	28 74
TRUE	PCIE_TBT_R2D_N<3..0>	28 74
TRUE	PCIE_TBT_D2R_C_P<3..0>	28 74
TRUE	PCIE_TBT_D2R_C_N<3..0>	28 74

TRUE	DMI_S2N_P<3..1>	5 12 74
TRUE	DMI_S2N_N<3..1>	5 12 74
TRUE	DMI_N2S_P<3..1>	5 12 74
TRUE	DMI_N2S_N<3..1>	5 12 74

PLACEABLE BEAD-PROBES FOR TBT

TBT_A_R2D_C_P<1>	1	SM BEAD-PROBE	BPA535 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_P<1>	1	SM BEAD-PROBE	BPA531 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	1	SM BEAD-PROBE	BPA532 NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_P<3:0>	5 12 72
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_N<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_P<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_N<3:0>	5 12 72
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 71
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 72
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 72
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 71
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 71
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 71
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 71
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 71
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 71
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 71
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 41
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 41 42 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTL	PM_THRMTRIP_L	6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	22 25 26 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 70
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 72
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 72
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 70
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 70

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 67 70
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 67 70
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 71
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 71

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	68 70 71
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	5 68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	5 68 70 71
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 28 70
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 28 70
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 28 70
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 28 70
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
	DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 70
	DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 70
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
	DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 70
	DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 70

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 72
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 72
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 72
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 72
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 72
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 72
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 72
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 72
T213 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_85D	USB	USB_EXTA_P	13 38
	USB_85D	USB	USB_EXTA_N	13 38
T24	USB_85D	USB	USB_EXTA_MUXED_P	38
T24	USB_85D	USB	USB_EXTA_MUXED_N	38
T24	USB_85D	USB	USB_LT1_P	38
T24	USB_85D	USB	USB_LT1_N	38
	USB_85D	USB	NC_USB_EXTCP	13 72
	USB_85D	USB	NC_USB_EXTCN	13 72
T23	USB_85D	USB	NC_USB_SDP	13 72
T23	USB_85D	USB	NC_USB_SDN	13 72
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
	USB_85D	USB	NC_USB_SMCP	72
	USB_85D	USB	NC_USB_SMCN	72
T28	USB_85D	USB	NC_USB_6P	13 72
T28	USB_85D	USB	NC_USB_6N	13 72
T28	USB_85D	USB	NC_USB_7P	13 72
T28	USB_85D	USB	NC_USB_7N	13 72
	USB_85D	USB	USB_EXTB_P	13 68 71
	USB_85D	USB	USB_EXTB_N	13 68 71
T26	USB_85D	USB	NC_USB_EXTDP	13 72
T25	USB_85D	USB	NC_USB_EXTDN	13 72
	USB_85D	USB	USB_BT_P	13 34
	USB_85D	USB	USB_BT_N	13 34
	USB_85D	USB	USB_BT_CONN_P	34 71
	USB_85D	USB	USB_BT_CONN_N	34 71
T28	USB_85D	USB	NC_USB_IRP	13 72
T28	USB_85D	USB	NC_USB_IRN	13 72
T28	USB_85D	USB	USB_TPAD_P	13 39
T28	USB_85D	USB	USB_TPAD_N	13 39
T30	USB_85D	USB	USB_TPAD_R_P	39
T30	USB_85D	USB	USB_TPAD_R_N	39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
T22 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
T23 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
T23 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
T22 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 68 71
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 68 71
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	68 71
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	68 71
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 68
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 68
T28 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 72
T28 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 72
T28	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 72
T28	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 72
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 72
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 72
T29	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 72
T29	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 72

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T256 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
T255 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
T255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
T255 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
T253 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
T256	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41 50 71
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41 50 71
LPC_RESET_L	LPC_45S	LPC	LPCPLUS_RESET_L	20 50 71
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 22 44 63 68 71
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 22 44 63 68 71
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
	HDA_45S	HDA	HDA_BIT_CLK_R	11
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
	HDA_45S	HDA	HDA_SYNC_R	11
	HDA_45S	HDA	HDA_RST_R_L	11
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
	HDA_45S	HDA	HDA_SDOUT_R	11 19
	SPI_45S	SPI	SPI_CLK_R	13 50
SPI_CLK	SPI_45S	SPI	SPI_CLK	50
	SPI_45S	SPI	SPI_MOSI_R	13 50
SPI_MOSI	SPI_45S	SPI	SPI_MOSI	50
SPI_MISO	SPI_45S	SPI	SPI_MISO	13 50
	SPI_45S	SPI	SPI_CS0_R_L	13 50
SPI_CS0	SPI_45S	SPI	SPI_CS0_L	50
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 68 71
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 68 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 71
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
[180]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
[180]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
[179]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 71
[179]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 71
[87] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
[87] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
[87]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
[87]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
[87] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
[87] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
[87]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
[87]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 50 71
[240]	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
[249] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
[254] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
[255] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
[254] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
[254] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
[257] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
[257] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
[255] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
[257] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
[256] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
[256] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
[180]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 71
[179]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 71
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
[87]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
[87]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
[285] PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
[285]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
[87] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
[87] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
[87] PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
[87] PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
[80] PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 66 71
[80] PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 71
[87] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
[87] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
[80] PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 71
[80] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 71
[80] PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
[80] PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
[80] PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 71
[87] PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
[135] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>	13 35
[136] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>	13 35
[138] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>	13 35
[137] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>	13 35
[139]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>	35
[134]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>	35

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A 22 23 24 70 74
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A 22 23 24 70 74
		MEM_PWR	PP1V35_S3_MEM 23 24 25 26 46 69

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Memory Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0> 28 31 72
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0> 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 28 31
T802 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 28 31
T810 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 31
T811 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 31
T809 DP_TBTPA_ML	DP_85D	DISPLAYPORT	
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0> 28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0> 28 31
T813 TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1> 31
T814 TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1> 31
T815 TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1> 28 31 72
T816 TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1> 28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 31
T819 TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0> 28 32
T817 TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0> 28 32
T818 TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0> 32
T816 TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0> 32
T823 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 28 32
T822 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 28 32
T826 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 32
T824 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 32
T828 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 32
T829 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 32
T832 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 28 32
T830 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 28 32
T834 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 32
T836 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 32
T831 TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0> 32
T833 TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0> 32
T835 TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0> 28 32
T837 TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0> 28 32
T839 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1> 32
T838 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1> 32
T840 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1> 28 32
T841 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1> 28 32
T842 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P 32
T843 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N 32
T844 TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 28 32
T845 TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 28 32
T847 TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 32
T846 TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 28

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 36 37
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 36 37
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 36 37
161	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 36 37
162		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 37
163	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 36 37
164	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 36 37
165	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 36 37
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 36 37
166	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 36 37
167	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 36 37
168	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 36 37
169	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 36 37
170	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 36 37
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 36 37
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 36 37
127	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 36 37
128	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 36 37
129		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 37 71
130		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 37 71
131	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 36 37
132	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 36 37
133		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 37 71
134		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 37 71
135			S2_MEM_PWR	PP1V35_CAM 36 37
136			S2_MEM_PWR	PP0V675_CAM_VREF 36 37
137			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 37
138			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 37

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 71
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 71
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 71
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 71
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	41 44 56 57 71
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 71
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	47
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	46
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N	46 59
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_N	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	62
	THERM_1TO1_45S	THERM	P1V05S0_CS_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P	62
	THERM_1TO1_45S	THERM	P1V05S0_SENSE_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	28 48
	THERM_1TO1_45S	THERM	TBT_THERMD_N	48
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N	47

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
	AUDIODIFF	AUDIO	RSUBIN_P	53
	AUDIODIFF	AUDIO	RSUBIN_N	53
	AUDIODIFF	AUDIO	LSUBIN_P	53
	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
	DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
	DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
	DIFFPAIR	AUDIO	HS_MIC_P	51 54
	DIFFPAIR	AUDIO	HS_MIC_N	51 54
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53
SB_POWER			PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 71
SB_POWER			PP3V3_S0	60 66 67 11 12 13 14 15 17 19 59 29 33 35
SB_POWER			PP1V35_S3RS0_CPUDDR	36 44 45 46 47 48 49 51 52 55 60 71 8 8 10 21 65 66 69
GND			GND	

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Project Specific Constraints

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0067	COMMON PARTS,MLB,J45	J45_COMMON
985-0045	DEV BOM,MLB,J45	J45_DEVEL:ENG
639-4822	PCBA,MLB,BETTER,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600_S
639-4823	PCBA,MLB,BETTER,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600
639-4828	PCBA,MLB,BETTER,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600_S
639-4829	PCBA,MLB,BETTER,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600
639-4834	PCBA,MLB,BETTER,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600_S
639-4835	PCBA,MLB,BETTER,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600
639-4840	PCBA,MLB,BEST,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600_S
639-4841	PCBA,MLB,BEST,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600
639-4846	PCBA,MLB,BEST,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600_S
639-4847	PCBA,MLB,BEST,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600
639-4852	PCBA,MLB,BEST,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600_S
639-4853	PCBA,MLB,BEST,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600
639-4858	PCBA,MLB,CTO,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600_S
639-4859	PCBA,MLB,CTO,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600
639-4864	PCBA,MLB,CTO,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600_S
639-4865	PCBA,MLB,CTO,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600
639-4870	PCBA,MLB,CTO,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600_S
639-4871	PCBA,MLB,CTO,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600

J45 BOM Groups

BOM GROUP	BOM OPTIONS
J45_COMMON	ALTERNATE,COMMON,J45_COMMON1,J45_COMMON2,J45_PROGPARTS
J45_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X16,S2_PWR:S0
J45_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45_PVB	BKLT:PROD,SENSOR_NONPROD:N
J45_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:DVT,TBTROM:PROG,TPAD_PSOC:PROG
J45_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,CAM_XTAL:YES
J45_DEVEL:FSB	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,SENSOR_NONPROD_R
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	CRW,SR18J,,PRQ,C0,2.0,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	CRW,SR18H,PRQ,C0,2.3,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	CRW,SR1BS,PRQ,C0,2.6,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QEWV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600_S	HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600_S	SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600_S	ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600_S	MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600	SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600	ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0067	1	J45 MLB BASE BOM	BASE	CRITICAL	BASE_BOM
985-0045	1	J45 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC_MASTER=J15_MLB SYNC_DATE=10/25/2012

PAGE TITLE: BOM Configuration

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Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S3919	1	IC,EPROM,Falcon RIDGE(V13.9)J44/45	U2890	CRITICAL	TBTROM:PROG
337S4587	1	IC,TP PSOC, QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK
341S3856	1	IC,TRKPD/KYBD,PSOC(V225)	U4801	CRITICAL	TPAD_PSOC:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3902	1	IC,SMC-B1,EXT,V2.12A54,EVT,J45	U5000	CRITICAL	SMC_PROG:EVT
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK:MACRONIX
335S0812	1	IC,SPI SRL 50MHZ,FLASH,64MBIT,SOIC8	U6100	CRITICAL	BOOTROM_BLANK:NUMONYX
341S3763	1	IC,EFI ROM(VXXXX)PROTO 0,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3780	1	IC,EFI ROM(V0035)PRE-PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PRE-PROTO1
341S3793	1	IC,EFI ROM(V0041)PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3811	1	IC,EFI ROM(V00xx)PROTO 2,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3890	1	IC,EFI ROM(V0100)PROTO3-J45 &EVT-J45	U6100	CRITICAL	BOOTROM_PROG:EVT
341S3929	1	IC,EFI ROM(Vxxxx)DVT-J45	U6100	CRITICAL	BOOTROM_PROG:DVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7845	1	MBP BARCODE LABEL	LABEL	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0241		ALL	Cyntec alt to TFT
376S1032	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Elpida F die alt
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba (U2030, U7001)

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PAGE TITLE: BOM Configuration

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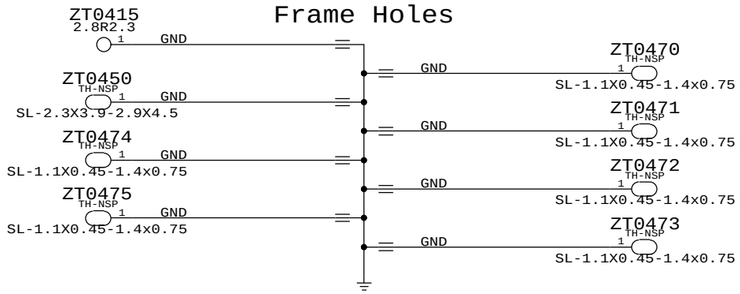
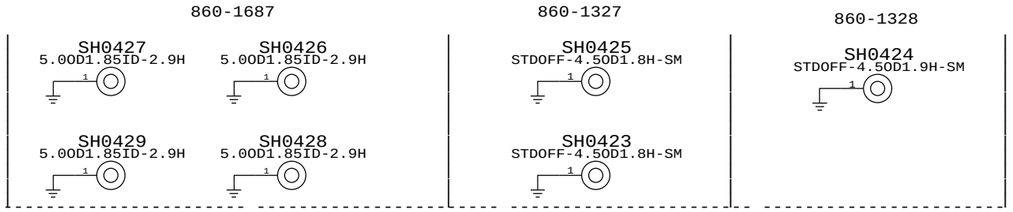
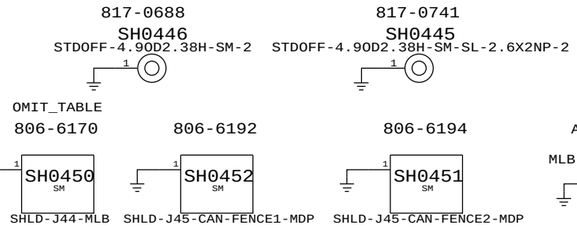
Frame Holes



J45 THERMAL MODULE STANDOFF





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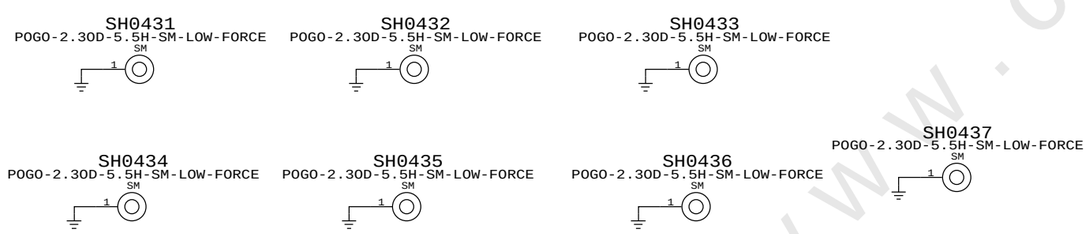
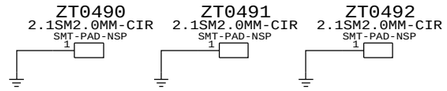
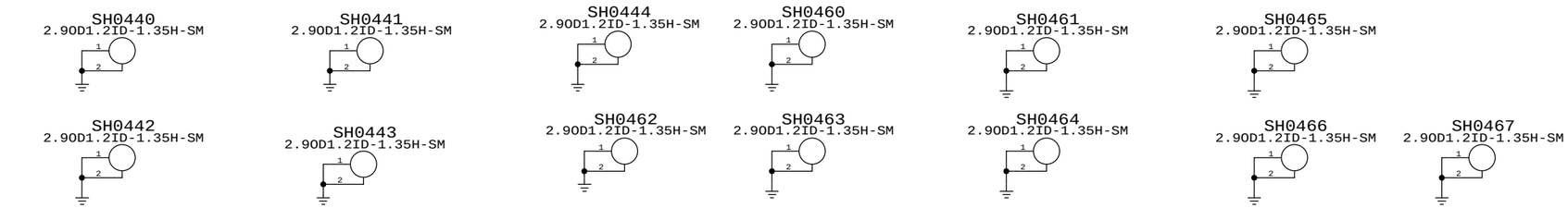


SMT GND TEST PONTS



J45 StAND OFF

860-1448



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
725-1807	1	INSULATOR,REAR,MLB,J45	REAR_INSULATOR	CRITICAL	
725-1877	1	INSULATOR,CPU,J45	CPU_INSULATOR	CRITICAL	
725-1787	1	INSULATOR,PCH,J15	PCH_INSULATOR	CRITICAL	
806-6193	2	CAN COVER,mDP	CAN_COVER1, CAN_COVER2	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
806-9391	1	SHIELD CAN, USB,J45	SH0450	CRITICAL	

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PAGE TITLE: PD Parts

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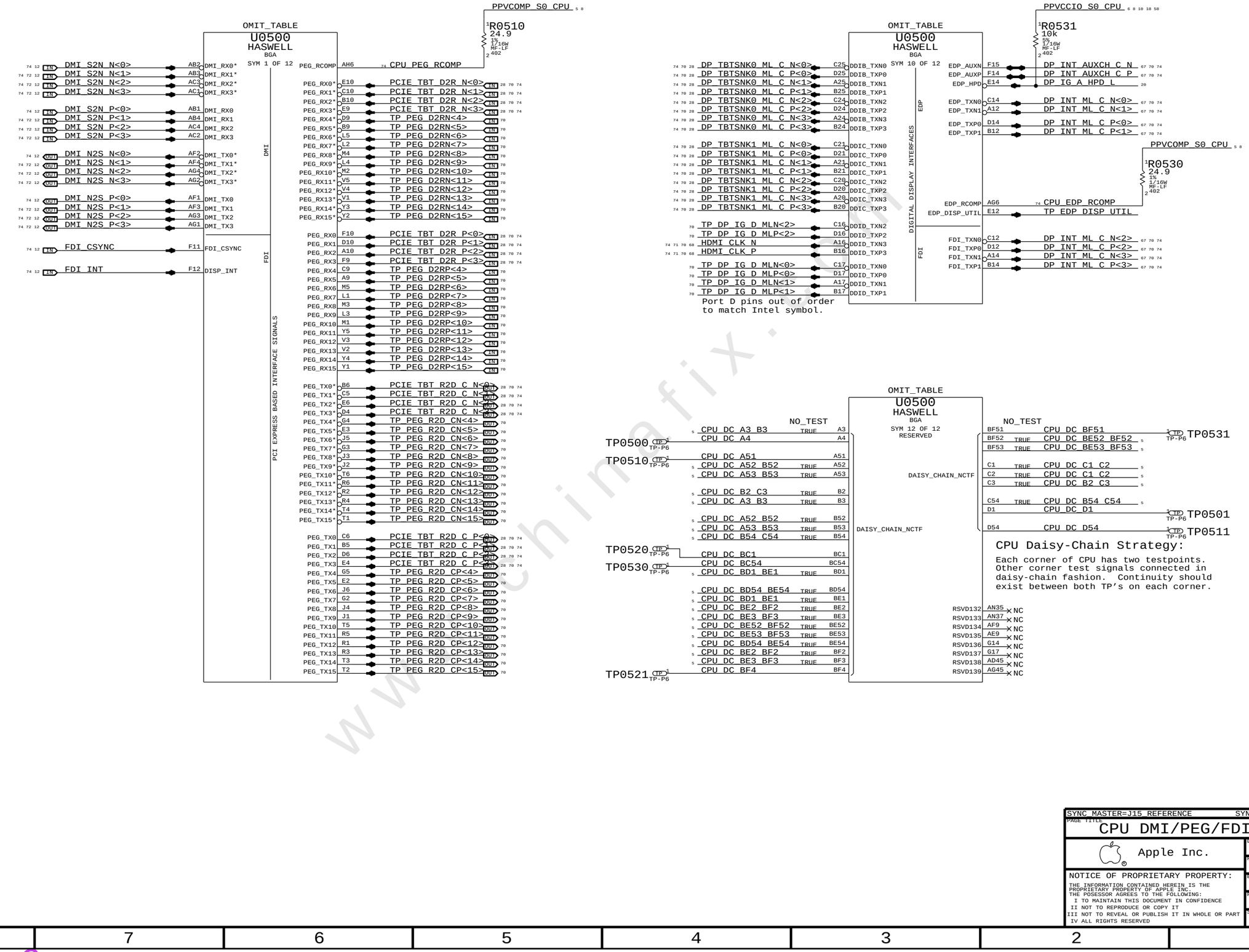

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PAGE TITLE

CPU DMI/PEG/FDI/RSVD

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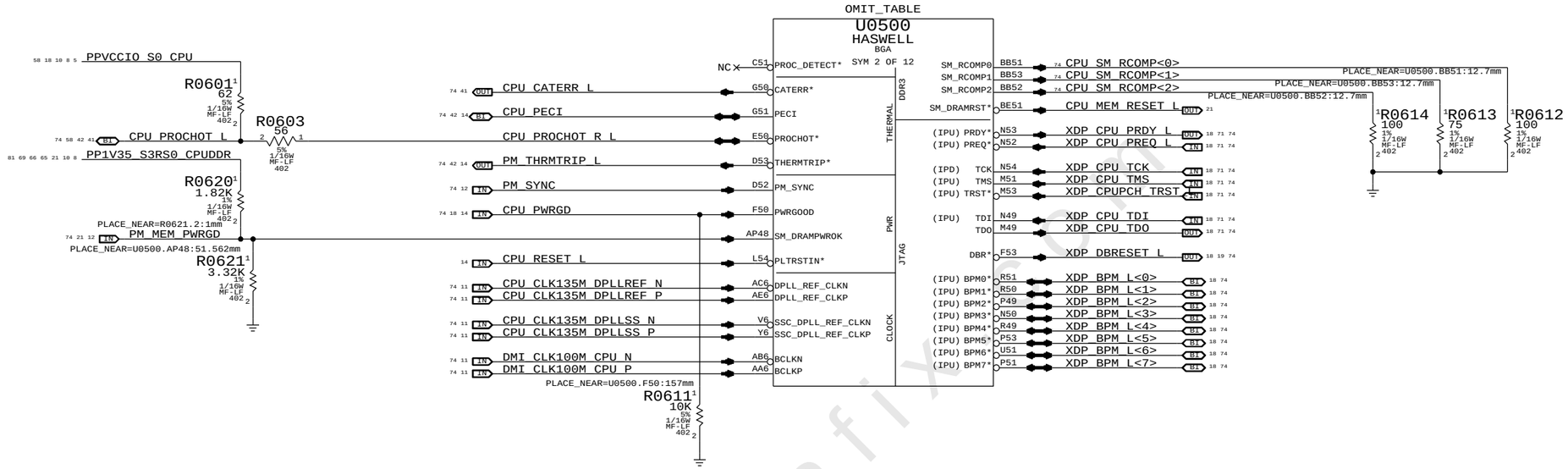
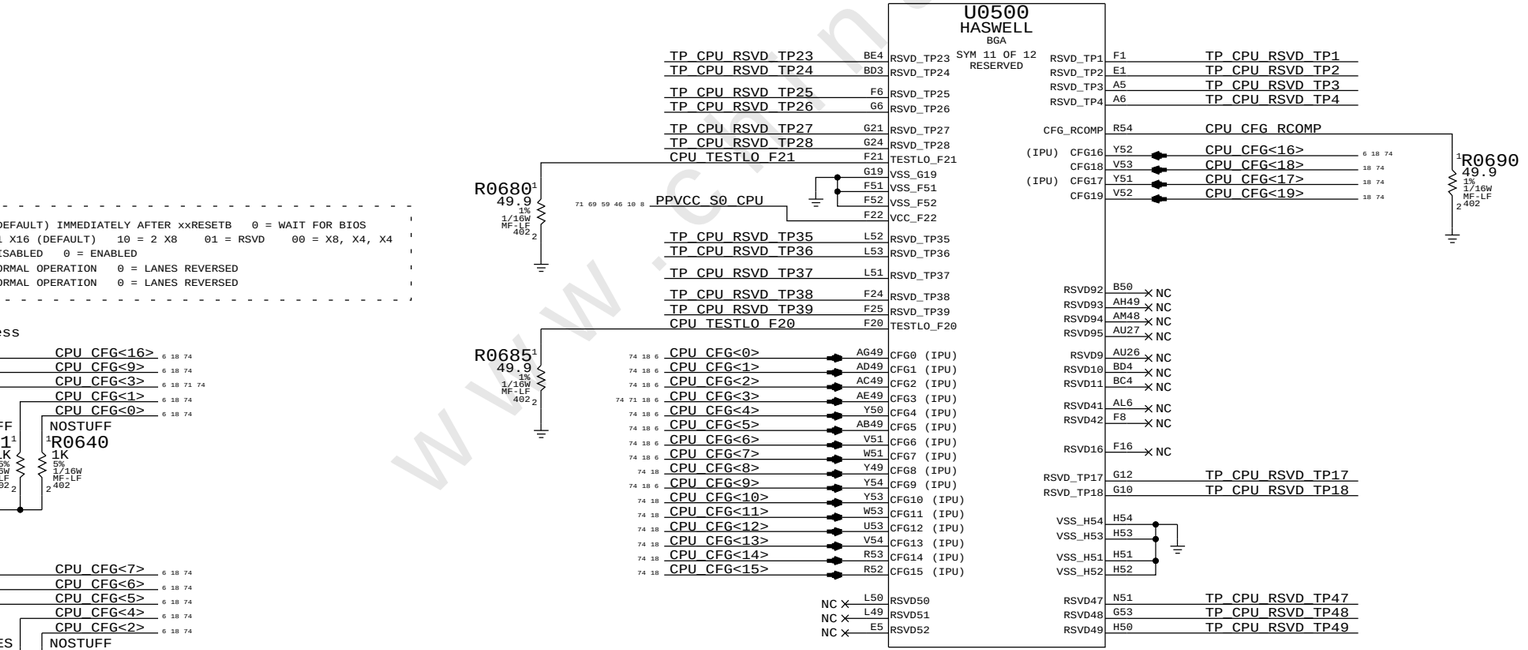
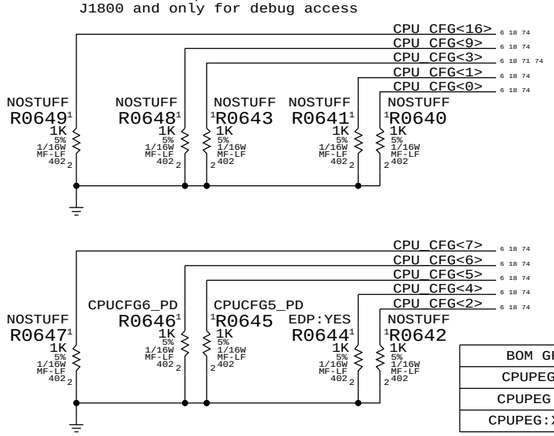





```
CFG [7] :PEG DEFER TRAINING              1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION              11 = 1 X16 (DEFAULT)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE              1 = DISABLED   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL           1 = NORMAL OPERATION   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL          1 = NORMAL OPERATION   0 = LANES REVERSED
```

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

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PAGE TITLE: CPU Clock/Misc/JTAG/CFG

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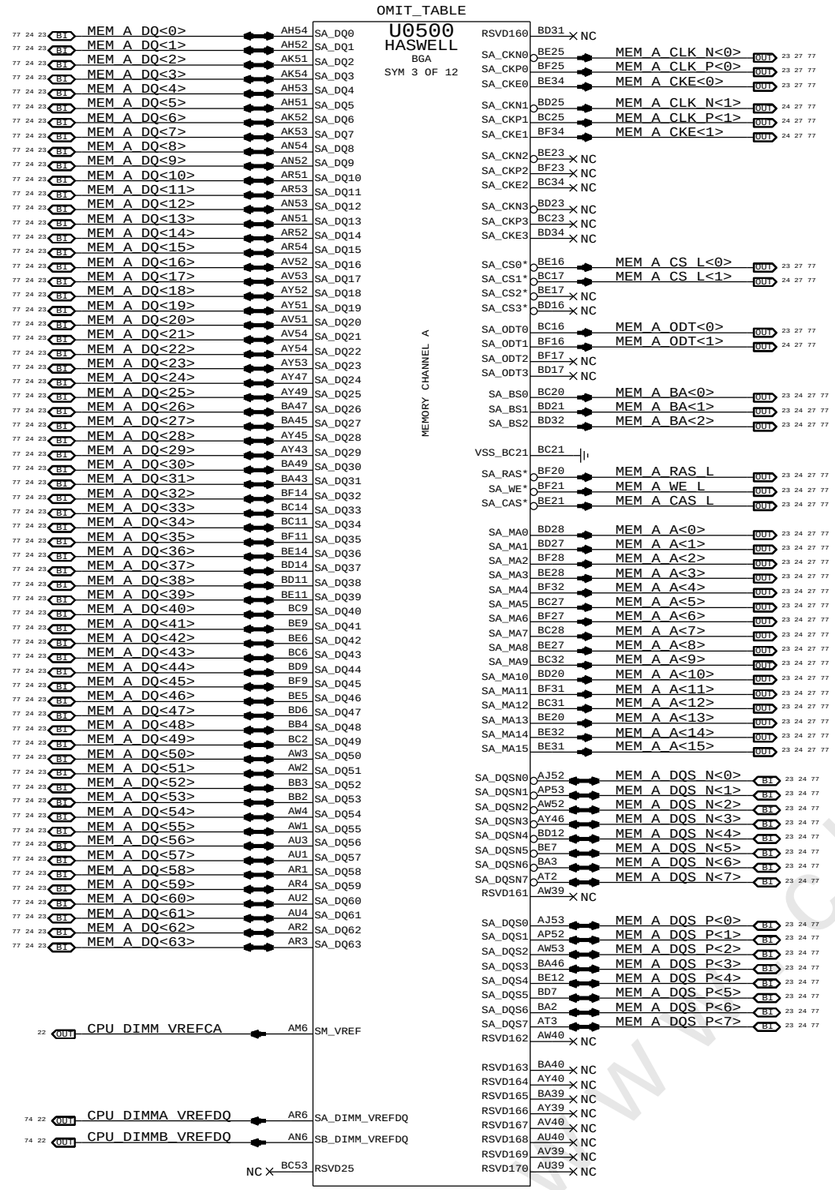

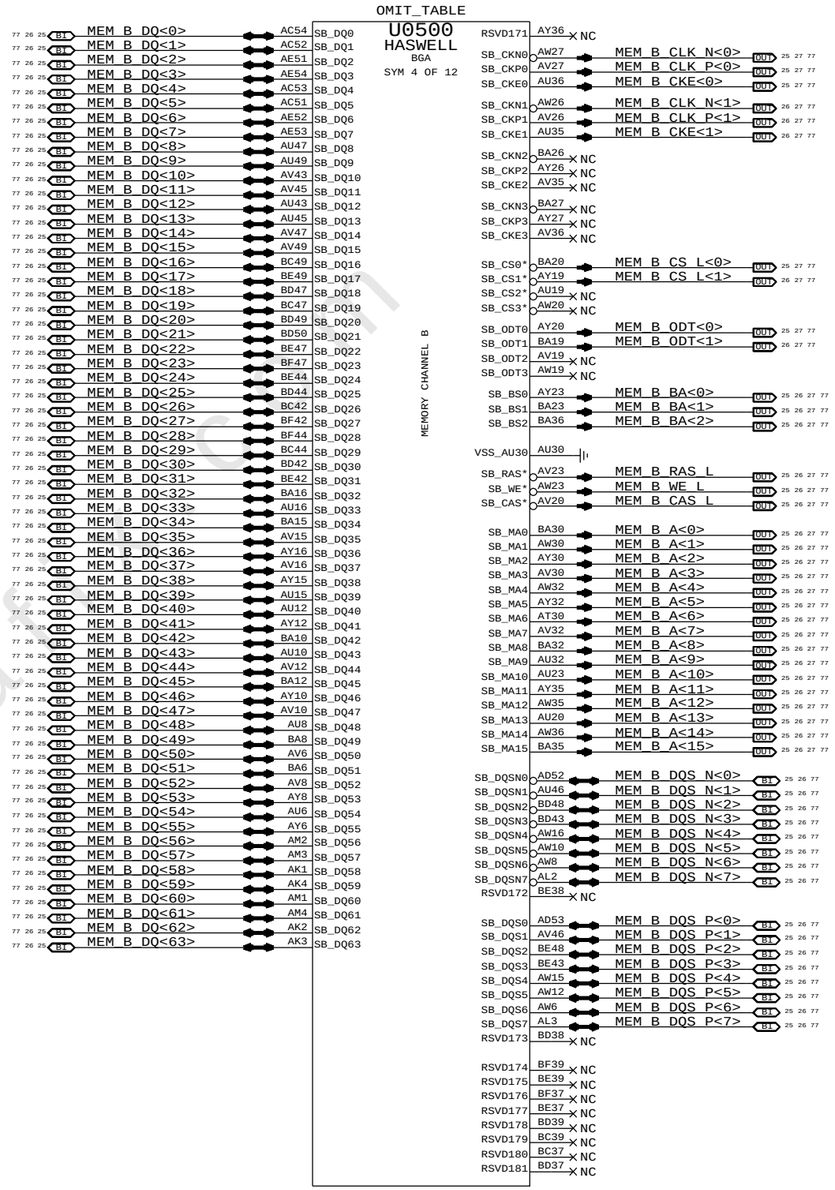

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PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

PP1V35_S3RS0_CPUDDR (81 69 66 65 21 10 6)

PPVCC_S0_CPU (71 69 59 46 10 8 6)

PPVCCIO_S0_CPU (50 10 10 6 5)
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

PPVCOMP_S0_CPU (5)
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

R0860 100 5% 1/10W MF-LF 402
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM

CPU_VCCSENSE_P (74 58) OUT

R0800 75 1% 1/10W MF-LF 402

R0802 110 1% 1/16W MF-LF 402

R0810 43 5% 1/16W MF-LF 402

R0811 0 5% 1/16W MF-LF 402

R0812 0 5% 1/16W MF-LF 402

CPU_VIDALERT_L (74 58) IN
CPU_VIDSCLK (74 58) OUT
CPU_VIDSOUT (74 58) BI

R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R

CPU_PWR_DEBUG (18) IN

TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
TP_CPU_IVR_ERROR
TP_CPU_RSVD_TP78

U0500
HASWELL
BGA
SYM 5 OF 12
OMIT_TABLE

NC	J17	RSVD64
NC	J21	RSVD65
NC	J26	RSVD66
NC	J31	RSVD67
	AR29	
	AR31	
	AR33	
	AT13	
	AT19	
	AT23	
	AT27	
	AT32	
	AT36	
	AV37	
	AW22	
	AW25	
	AW29	
	AW33	
	AY18	
	BB21	
	BB22	VDDQ
	BB26	
	BB27	
	BB30	
	BB31	
	BB34	
	BB36	
	BD22	
	BD26	
	BD30	
	BD33	
	BE18	
	BE22	
	BE26	
	BE30	
	BE33	
NC	AN31	RSVD68
	L6	VCC_L6
	M6	VCC_M6
NC	AN22	RSVD69
NC	AN18	RSVD70
	C50	VCC_SENSE
NC	AH9	RSVD71
	D51	VCCIO_OUT
NC	F17	FC_F17
	AK6	VCOMP_OUT
NC	AN33	RSVD72
NC	W9	RSVD73
NC	J12	RSVD79(VSS)
NC	AR49	RSVD74
	J53	VIDALERT*
	J52	VIDSCLK
	J50	VIDSOUT
	B51	VSS_B51
	F19	PWR_DEBUG
	E52	VSS_E52
	V49	RSVD75
	U49	RSVD76
	AM49	IVR_ERROR
	W49	RSVD78
	V50	VSS_V50(RSVD)
	AN49	VSS_AN49(RSVD)
	AJ49	VSS_AJ49(RSVD)
	AG50	VSS_AG50(RSVD)
	AK49	VSS_AK49(RSVD)
	AJ50	VSS_AJ50(RSVD)
	AP49	VSS_AP49(RSVD)
	AB50	VSS_AB50(RSVD)
	AP50	VSS_AP50(RSVD)
	AD50	VSS_AD50(RSVD)
	AM50	VSS_AM50(RSVD)
	A36	
	A38	
	A39	
	A42	
	A43	
	A45	
	A46	VCC
	A48	
	AA46	
	AA47	
	AA8	
	AA9	

PPVCC_S0_CPU (6 8 10 46 59 69 71)

	B43	
	B45	
	B46	
	B48	
	C27	
	C28	
	C31	
	C32	
	C34	
	C36	
	C38	
	C39	
	C42	
	C43	
	C45	
	C46	
	C48	
	D27	
	D28	
	D31	
	D32	
	D34	
	D36	
	D38	
	D39	
	D42	
	D43	
	D45	
	D46	
	D48	
	E27	
	E28	
	E31	
	E32	
	E34	
	E36	
	E38	
	E39	
	E42	
	E43	
	E45	
	E46	
	E48	VCC
	F27	
	F28	
	F31	
	F32	
	F34	
	F36	
	F38	
	F39	
	F42	
	F43	
	F45	
	F46	
	F48	
	G27	
	G29	
	G31	
	G32	
	G34	
	G36	
	G38	
	G39	
	G42	
	G43	
	G45	
	G46	
	G48	
	H11	
	H12	
	H13	
	H14	
	H16	
	H17	
	H18	
	H19	
	H20	
	H21	
	H23	
	H24	
	H25	
	H26	
	H27	
	H29	

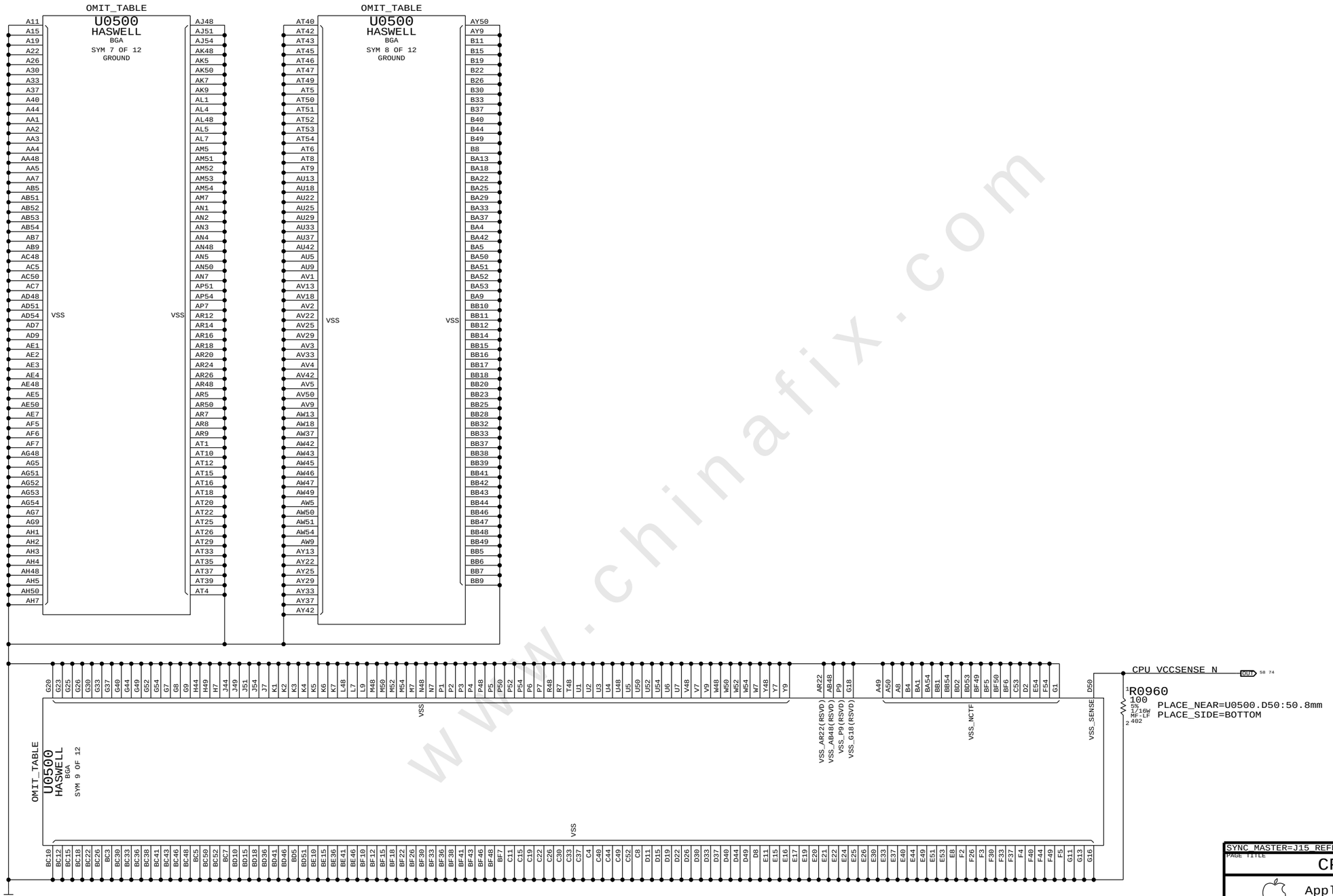
Connections would be required
for 2014 CPU support.

FC_D5	D5	TP_CPU_FC_VCCST
FC_D3	D3	TP_CPU_FC_VCCST_PWRGD

OMIT_TABLE
U0500
HASWELL
BGA
SYM 6 OF 12
POWER

VCC

| | | |



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CPU Ground

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 8x 210uF(2x nostuff) 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

71 60 59 46 8 6 PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 | C1001 1UF 10% 10V X6S-CERM 0402 | C1002 1UF 10% 10V X6S-CERM 0402 | C1003 1UF 10% 10V X6S-CERM 0402 | C1004 1UF 10% 10V X6S-CERM 0402 | C1005 1UF 10% 10V X6S-CERM 0402 | C1006 1UF 10% 10V X6S-CERM 0402 | C1007 1UF 10% 10V X6S-CERM 0402 | C1008 1UF 10% 10V X6S-CERM 0402 | C1009 1UF 10% 10V X6S-CERM 0402 | C1010 1UF 10% 10V X6S-CERM 0402 | C1011 1UF 10% 10V X6S-CERM 0402 | C1012 1UF 10% 10V X6S-CERM 0402 | C1013 1UF 10% 10V X6S-CERM 0402 | C1014 1UF 10% 10V X6S-CERM 0402 | C1015 1UF 10% 10V X6S-CERM 0402 | C1016 1UF 10% 10V X6S-CERM 0402 | C1017 1UF 10% 10V X6S-CERM 0402 | C1018 1UF 10% 10V X6S-CERM 0402 | C1019 1UF 10% 10V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

CAPs for Acoustic control (C109A-C102D)

C1020 20UF 20% 4V X5R-CERM 0402-2 | C1021 20UF 20% 4V X5R-CERM 0402-2 | C1022 20UF 20% 4V X5R-CERM 0402-2 | C1023 20UF 20% 4V X5R-CERM 0402-2 | C109A 20UF 20% 4V X5R-CERM 0402-2 | C109B 20UF 20% 4V X5R-CERM 0402-2 | C109C 20UF 20% 4V X5R-CERM 0402-2 | C109D 20UF 20% 4V X5R-CERM 0402-2 | C109E 20UF 20% 4V X5R-CERM 0402-2 | C109F 20UF 20% 4V X5R-CERM 0402-2 | C101A 20UF 20% 4V X5R-CERM 0402-2 | C101B 20UF 20% 4V X5R-CERM 0402-2 | C101C 20UF 20% 4V X5R-CERM 0402-2 | C101D 20UF 20% 4V X5R-CERM 0402-2 | C101E 20UF 20% 4V X5R-CERM 0402-2 | C101F 20UF 20% 4V X5R-CERM 0402-2 | C102A 20UF 20% 4V X5R-CERM 0402-2 | C102B 20UF 20% 4V X5R-CERM 0402-2 | C102C 20UF 20% 4V X5R-CERM 0402-2 | C102D 20UF 20% 4V X5R-CERM 0402-2

NO STUFF NO STUFF

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

CRITICAL C1024 20UF 20% 4V X5R-CERM 0402-2 | C1025 | C1026 | C1027 | C1028 | C1029 | C1030 | C1031 | C1032 | C1033 | C1034 | C1035 | C1036 | C1037 | C1038 | C1039 | C1040 | C1041 | C1042 | C1043 | C1044 | C1045

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

CRITICAL C1046 20UF 20% 4V X5R-CERM 0402-2 | C1047 | C1048 | C1049 | C1050 | C1051 | C1052 | C1053 | C1054 | C1055 | C1056 | C1057 | C1058 | C1059 | C1060 | C1061 | C1062 | C1063 | C1064 | C1065 | C1066 | C1067

PLACEMENT_NOTE (C1068-C1076:

NO STUFF NO STUFF

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S | C1069 | C1070 | C1071 | C1072 | C1073 | C1074 | C1075 | C1076 | C1077 210UF 20% 2.5V POLY-TANT CASE-B2S

CAPs for Acoustic control (C102E-C103F)

NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF

C102E 20UF 20% 4V X5R-CERM 0402-2 | C102F | C103A | C103B | C103C | C103D | C103E | C103F

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

66 65 21 8 6 81 80 PP1V35_S3RS0_CPUDDR

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402 | C1081 1UF 10% 10V X6S-CERM 0402 | C1082 1UF 10% 10V X6S-CERM 0402 | C1083 1UF 10% 10V X6S-CERM 0402 | C1084 1UF 10% 10V X6S-CERM 0402 | C1085 1UF 10% 10V X6S-CERM 0402 | C1086 1UF 10% 10V X6S-CERM 0402 | C1087 1UF 10% 10V X6S-CERM 0402 | C1088 1UF 10% 10V X6S-CERM 0402 | C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603 | C1091 10UF 20% 4V X6S-CERM 0603 | C1092 10UF 20% 4V X6S-CERM 0603 | C1093 10UF 20% 4V X6S-CERM 0603 | C1094 10UF 20% 4V X6S-CERM 0603 | C1095 10UF 20% 4V X6S-CERM 0603 | C1096 10UF 20% 4V X6S-CERM 0603 | C1097 10UF 20% 4V X6S-CERM 0603

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 2.5V POLY-TANT D1ST-ECGLT-COMBO

CRITICAL C1099 330UF-6MOHM 20% 2.5V POLY-TANT D1ST-ECGLT-COMBO

(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

58 18 8 6 5 PPVCCIO_S0_CPU

C1079 0.01UF 10% 10V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

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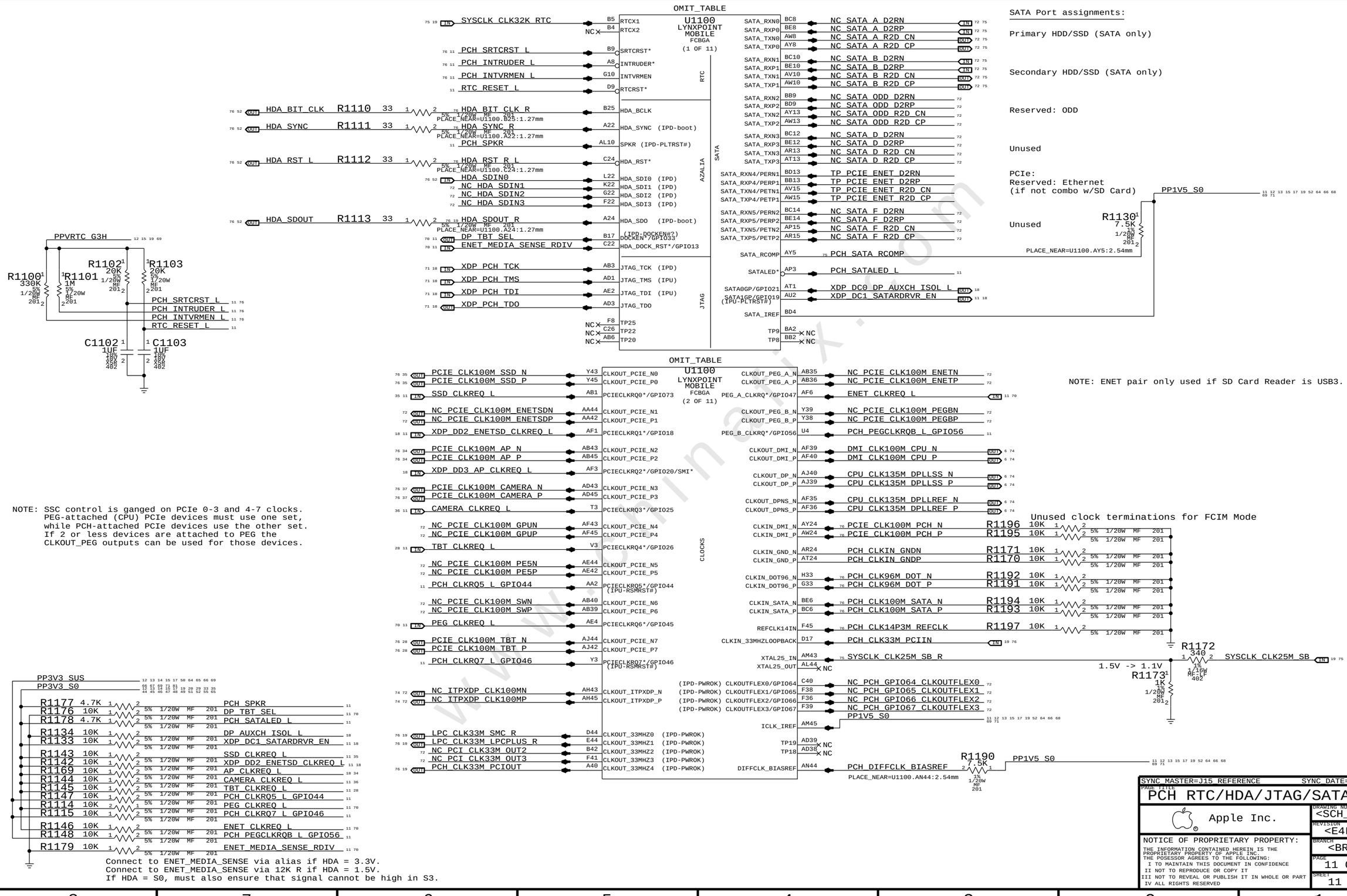

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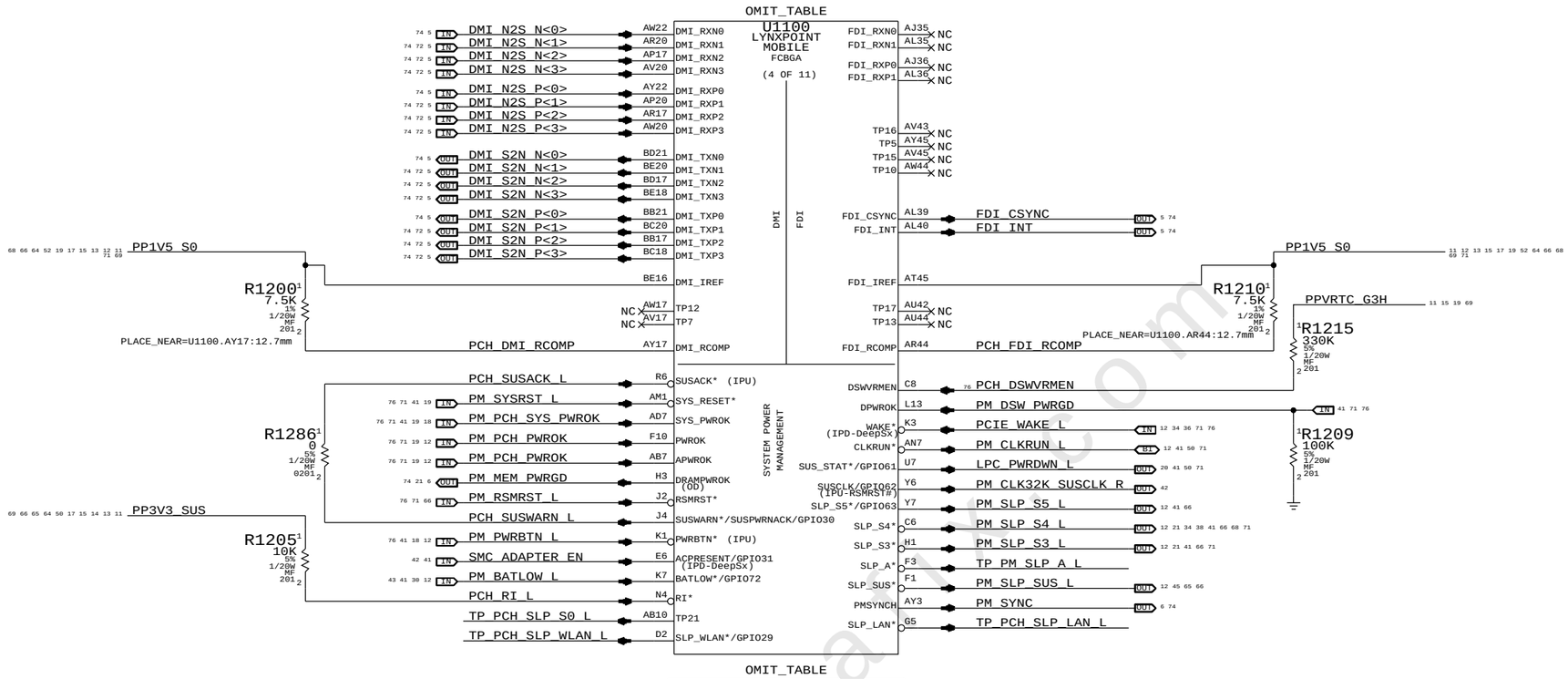

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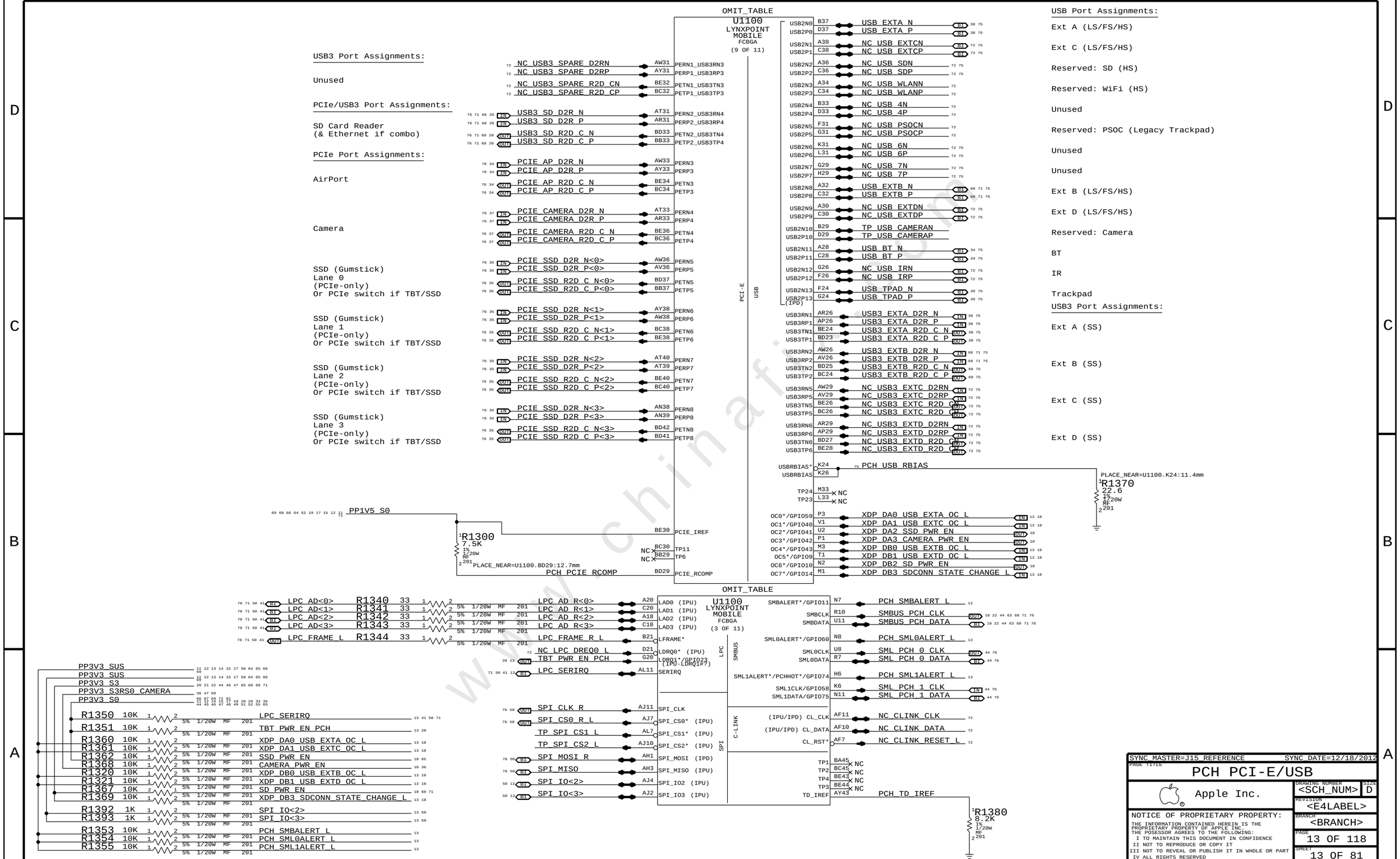

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Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(6 OF 11)

GPIO

28 20	IN	TBT_CIO_PLUG_EVENT_L	AT8 BMBUSY*/GPIO0
70 14	IN	FW_PME_L	F13 TACH1/GPIO1
70 14	IN	DPMUX_UC_IRQ	A14 TACH2/GPIO6
41 14	IN	SMC_RUNTIME_SCI_L	G15 TACH3/GPIO7
18	OUT	XDP_FC0_HDD_PWR_EN	Y1 GPIO8 (IPU-RSMRST#)
70 14	OUT	WOL_EN	K13 LAN_PHY_PWR_CTRL/GPIO12
70 14	OUT	MEM_VDD_SEL_1V5_L	AB11 GPIO15
18 14	IN	XDP_DD0_SSD_PCIE_SEL_L	AN2 SATA4GP/GPIO16 (IPU-BOOT/SATA4GP?)
71 50 14	BI	LPCPLUS_GPIO	C14 TACH0/GPIO17
20 14	OUT	JTAG_TBT_TMS_PCH	BB4 SCLOCK/GPIO22
70 14	BI	TBT_GO2SX_BIDIR	Y10 GPIO24
41 14	IN	SMC_WAKE_SCI_L	R11 GPIO27 (IPU-DeepSx)
21	OUT	ISOLATE_CPU_MEM_L	AD11 GPIO28
20	OUT	TBT_POC_RESET_L	AN6 GPIO34
18	OUT	XDP_FC1_GPU_GOOD	AP1 GPIO35/NMI*
18 14	OUT	XDP_DC2_ODD_PWR_EN_L	AT3 SATA2GP/GPIO36 (IPD-PLTRST#)
18	OUT	XDP_DC3_JTAG_ISP_TCK	AK1 SATA3GP/GPIO37 (IPD-PLTRST#)
20 14	IN	JTAG_ISP_TDO	AT7 SLOAD/GPIO38
20 14	OUT	JTAG_ISP_TDI	AM3 SDATAOUT0/GPIO39
70 14	OUT	FW_PWR_EN_PCH	AN4 SDATAOUT1/GPIO48
		XDP_DD1_MLB_RAMCFG1	AK3 SATA5GP/GPIO49 (IPU-BOOT/SATA5GP?)
71 50 14	BI	SPIROM_USE_MLB	U12 GPIO57
20		MLB_RAMCFG3	C16 TACH4/GPIO68
20		MLB_RAMCFG2	D13 TACH5/GPIO69
20	IN	SD_SEL_PCIE_L_USB_H	G13 TACH6/GPIO70 (IPU-BOOT?)
20		MLB_RAMCFG0	H15 TACH7/GPIO71 (IPU-BOOT?)

CPU/MISC

TP14	AN10	PCH_A20GATE 14
(IPD) PECI	AY1	PCH_PECI
RCIN*	AT6	PCH_RCIN_L 14 76
PROCPWRGD	AV3	PCH_PROCPWRGD
THRMTRIP*	AV1	PM_THRMTRIP_L_R 15 42
PLTRST_PROC*	AU4	CPU_RESET_L OUT 6
VSS	N10	
	A2	
	A41	
	A43	
	A44	
	B1	
	B2	
	B44	
	B45	
	BA1	
	BC1	
	BD1	
VSS	BD2	
	BD44	
	BD45	
	BE2	
	BE3	
	D1	
	E1	
	E45	
	A4	
	BE41	
	BE5	
	C45	VSS
	A5	

PP1V05_S0 15 17 18 42 62 66 69 71
NO STUFF
R1457 1K 5% 1/16W MF-LF 402

NO STUFF
R1470 43 5% 1/20W MF 201 — CPU_PECI BI 6 42 74
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD OUT 6 18 74
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L IN 6 42 74

PP3V3_S0
RAMCFG0:H R1475 10K 5% 1/20W MF 201
RAMCFG1:H R1474 10K 5% 1/20W MF 201
RAMCFG2:H R1473 10K 5% 1/20W MF 201
RAMCFG3:H R1472 10K 5% 1/20W MF 201

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PP3V3_S5
PP3V3_SUS
PP3V3_S0

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	1 2	FW_PME_L 14 70
R1411	20K	2 1	DPMUX_UC_IRQ 14 70
R1496	10K	1 2	SMC_RUNTIME_SCI_L 14 41
R1494	10K	1 2	WOL_EN 14 70
R1489	10K	1 2	MEM_VDD_SEL_1V5_L 14 70
R1495	100K	2 1	XDP_DD0_SSD_PCIE_SEL_L 14 18
R1490	100K	1 2	LPCPLUS_GPIO 14 50 71
R1412	10K	2 1	JTAG_TBT_TMS_PCH 14 20
R1492	10K	1 2	TBT_GO2SX_BIDIR 14 70
R1491	10K	1 2	SMC_WAKE_SCI_L 14 41
R1498	10K	2 1	XDP_DC2_ODD_PWR_EN_L 14 18
R1413	10K	2 1	JTAG_ISP_TCK 18 20
R1486	10K	1 2	JTAG_ISP_TDO 14 20
R1499	10K	1 2	JTAG_ISP_TDI 14 20
R1484	10K	1 2	FW_PWR_EN_PCH 14 70
R1493	100K	1 2	SPIROM_USE_MLB 14 50 71

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K	1 2	PCH_A20GATE 14
R1455	10K	1 2	PCH_RCIN_L 14 76

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PAGE TITLE: PCH GPIO/MISC/NCTF

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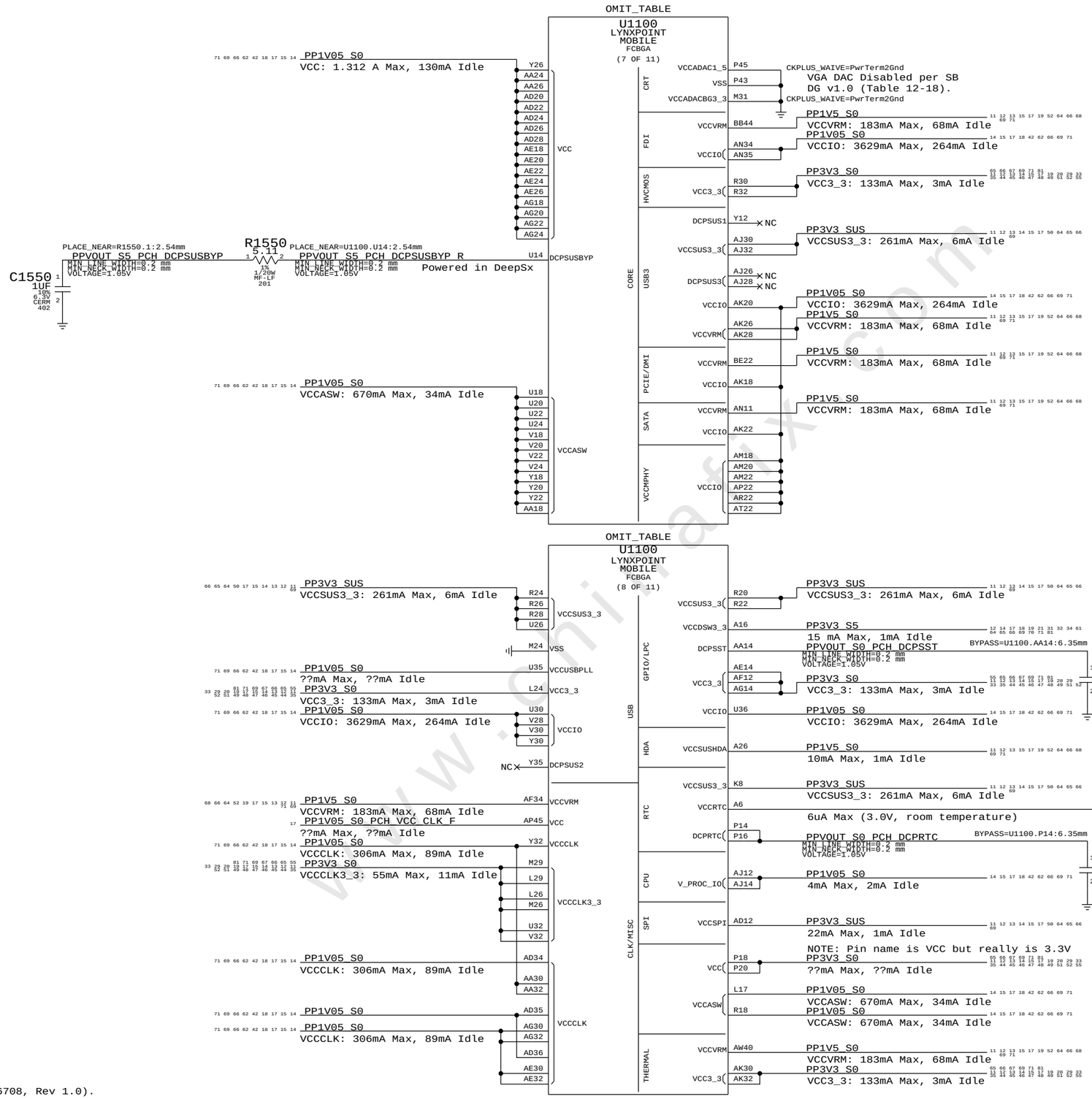

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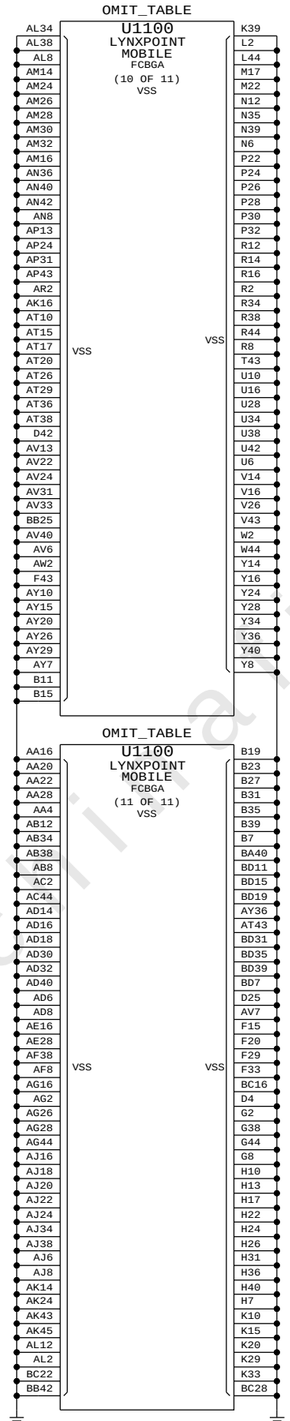

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PCH Grounds

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.A16:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD12:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1704 0.1UF 20% 10V CERM 402
BYPASS=U1100.R20:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS

C1706 0.1UF 20% 10V CERM 402
BYPASS=U1100.R26:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.K8:6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0

C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.L26:6.35mm
BYPASS=U1100.L29:6.35mm
BYPASS=U1100.M29:6.35mm
BYPASS=U1100.U32:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0

C1726 0.1UF 20% 10V CERM 402
BYPASS=U1100.R30:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0

C1730 0.1UF 20% 10V CERM 402
BYPASS=U1100.L24:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1732 0.1UF 20% 10V CERM 402
BYPASS=U1100.AK30:6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0

C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.P18:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle

C1750 22UF 20% 6.3V X5R-CERM-1 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1755 10UF 20% 6.3V X5R 603
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.AG18:12.7mm
BYPASS=U1100.AG22:6.35mm
BYPASS=U1100.AP20:6.35mm
BYPASS=U1100.AE18:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0

C1760 10UF 20% 6.3V X5R 603
C1761 1UF 10% 6.3V CERM 402
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.AK18:12.7mm
BYPASS=U1100.AK18:6.35mm
BYPASS=U1100.AK22:6.35mm
BYPASS=U1100.AK20:6.35mm
BYPASS=U1100.AM18:6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0

C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.U35:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0

C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.AN34:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1774 0.1UF 20% 10V CERM 402
BYPASS=U1100.U30:6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0

C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.AJ12:12.7mm
BYPASS=U1100.AJ12:6.35mm
BYPASS=U1100.AJ12:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0

C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AE30:6.35mm
BYPASS=U1100.AG30:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0

C1778 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD35:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0

C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD34:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0

C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA30:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0

C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.A26:6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

C1740 10UF 20% 6.3V X5R 603
BYPASS=U1100.AF34:12.7mm

PP1V05_S0
??mA Max, ??mA Idle

R1790 1 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603

PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V

NO STUFF
C1790 10UF 20% 6.3V X5R 603
C1791 1UF 10% 10V X5R 402
BYPASS=U1100.AP45:12.7mm
BYPASS=U1100.AP45:6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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PCH DECOUPLING

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807
(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

PP1V05_S0 → R1830 150 5% 1/16W MF-LF 402

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	XDP_CPU_PRESENT_L

CPU_PWRGD → R1800 1K XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.F50:2.54mm
PM_PWRBTN_L → R1802 0 XDP 5% 1/20W MF 0201 PLACE_NEAR=U5000.J3:2.54mm
PM_PCH_SYS_PWROK → R1804 0 XDP 5% 1/16W MF-LF 402

XDP_CPU_TCK → R1820 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.M49:28mm
XDP_CPU_TCK → R1823 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.N54:28mm
XDP_CPUPCH_TRST_L → R1824 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.M53:28mm
PP1V05_S0

TDI and TMS are terminated in CPU.

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

XDP_CPU_PRESENT_L

R1805 1K XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.A67:2.54mm
PLT_RESET_L
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563
XDP_CPU_TDO PLACE_NEAR=J1800.51:28mm

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563
XDP_CPUPCH_TRST_L MAKE_BASE=TRUE PLACE_NEAR=J1800.53:28mm

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563
XDP_CPU_TDI PLACE_NEAR=J1800.55:28mm

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563
XDP_CPU_TMS PLACE_NEAR=J1800.57:28mm

PCH/XDP Signals

		OMIT (All 10 R's)	Non-XDP Signals
XDP_DA0_USB_EXTA_OC_L	R1890	SHORT	USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895	SHORT	SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893	SHORT	CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894	SHORT	USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896	SHORT	SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897	SHORT	SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872	SHORT	DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN	MAKE_BASE=TRUE		XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L	MAKE_BASE=TRUE		XDP_DC2_ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875	SHORT	JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876	SHORT	SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1	MAKE_BASE=TRUE		XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L	MAKE_BASE=TRUE		XDP_DD2_ENETSD_CLKREQ
XDP_DD3_AP_CLKREQ_L	R1879	SHORT	AP_CLKREQ_L

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813
(TP-P6)

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, NC)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS
XDP_PCH_TDO → R1860 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U1100.AD3:28mm
XDP_PCH_TDI → R1861 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U1100.AE2:28mm
XDP_PCH_TMS → R1862 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U1100.AD1:28mm
XDP_PCH_TCK → R1866 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U1100.AB3:28mm

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: CPU & PCH XDP

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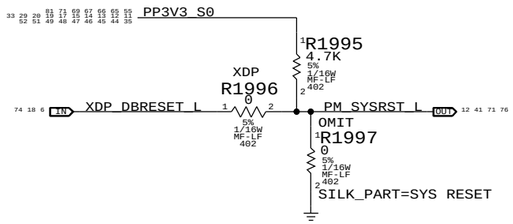
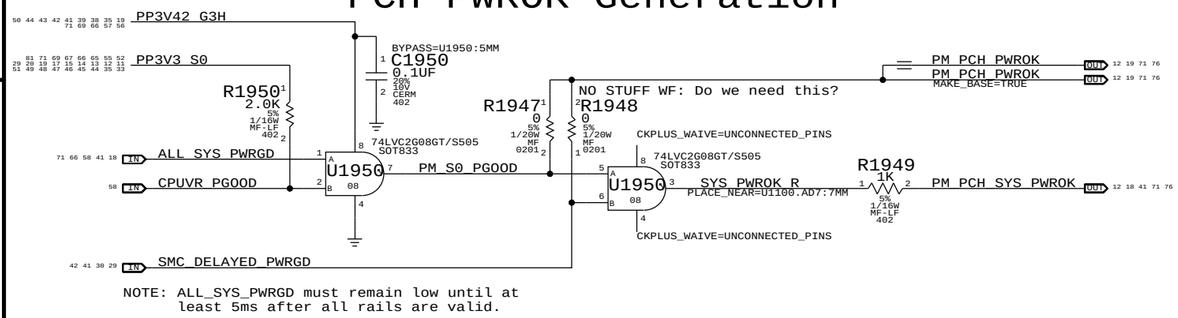
PCH Reset Button

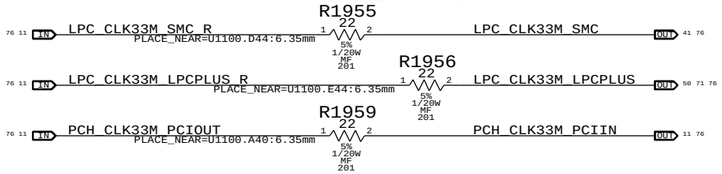


PCH PWROK Generation



NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

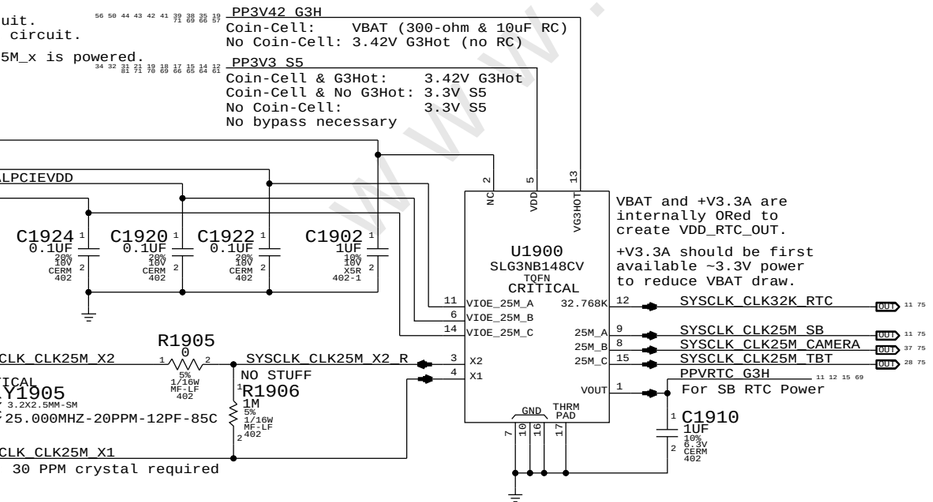
PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenClk 25MHz Power — PP3V3_S5

SB XTAL Power — PP1V5_S0
Camera XTAL Power — PP1V2_CAM_XTALPCIEVDD
TBT XTAL Power — PP3V3_TBTLC

NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).



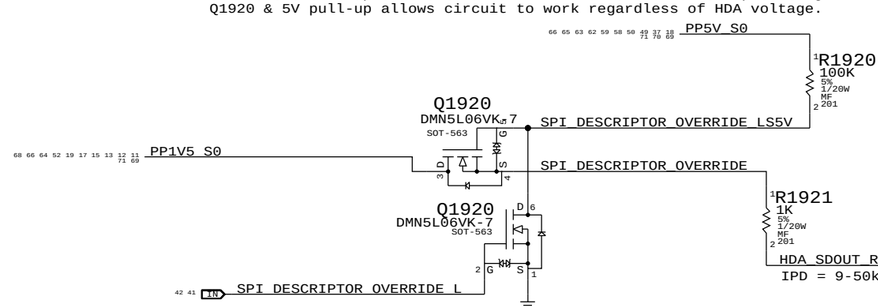
VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

NOTE: 30 PPM crystal required

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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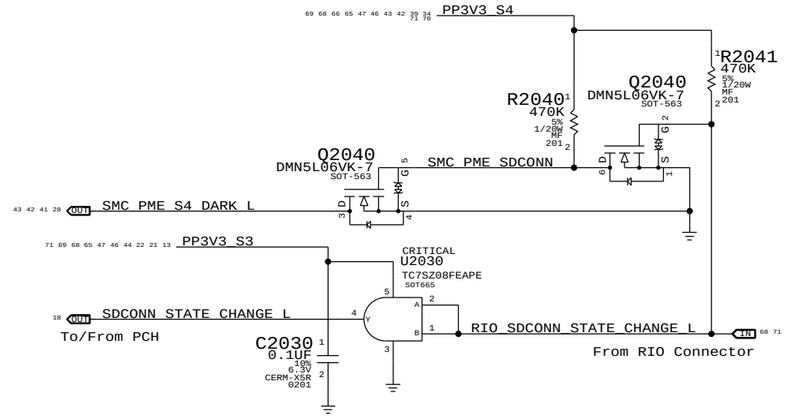
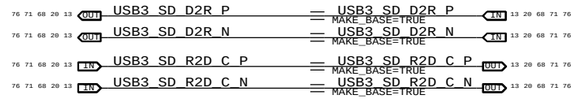
RIO SD Card Reader Support



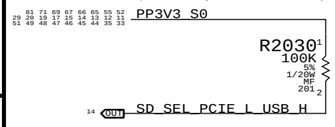
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



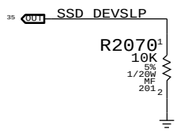
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe



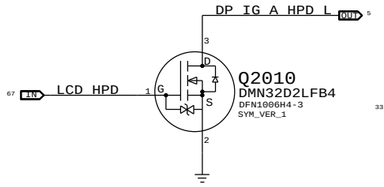
GS3 Connector Support

DEVSLP not supported on LPT-H

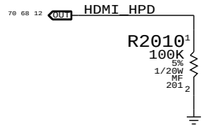


LCD HPD Inverter

(Pull-Up on CPU Page)

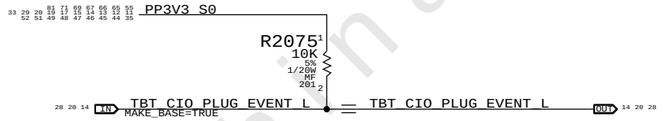


HDMI HPD pull-down



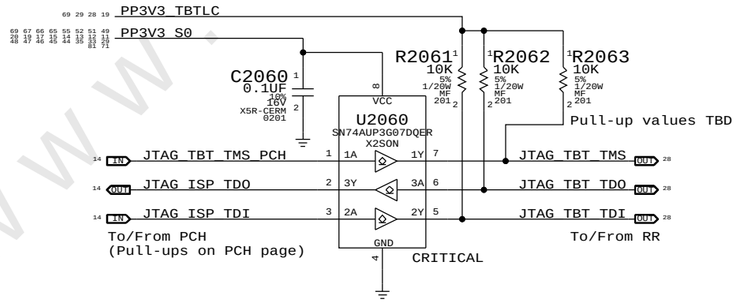
Redwood Ridge Support

RR output is open-drain, no isolation necessary

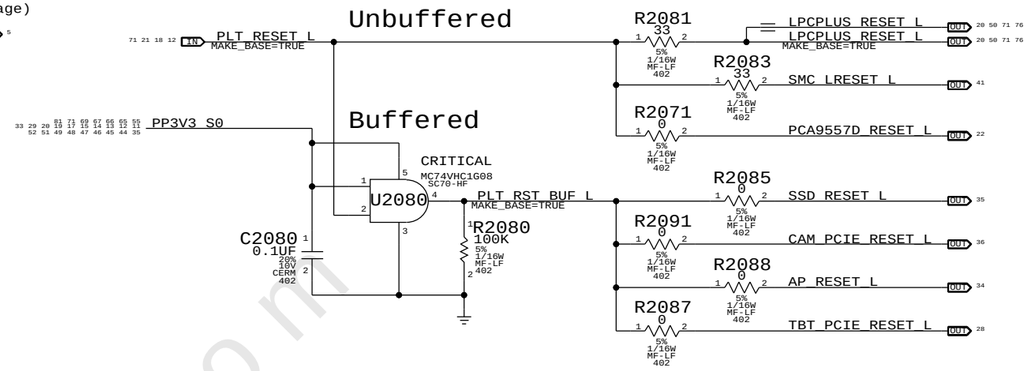


Redwood Ridge JTAG Isolation

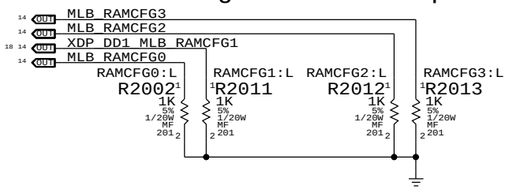
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



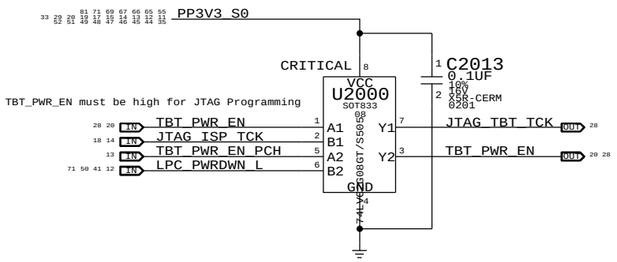
Platform Reset Connections



RAM Configuration Straps



GPIO Glitch Prevention



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PAGE TITLE: Project Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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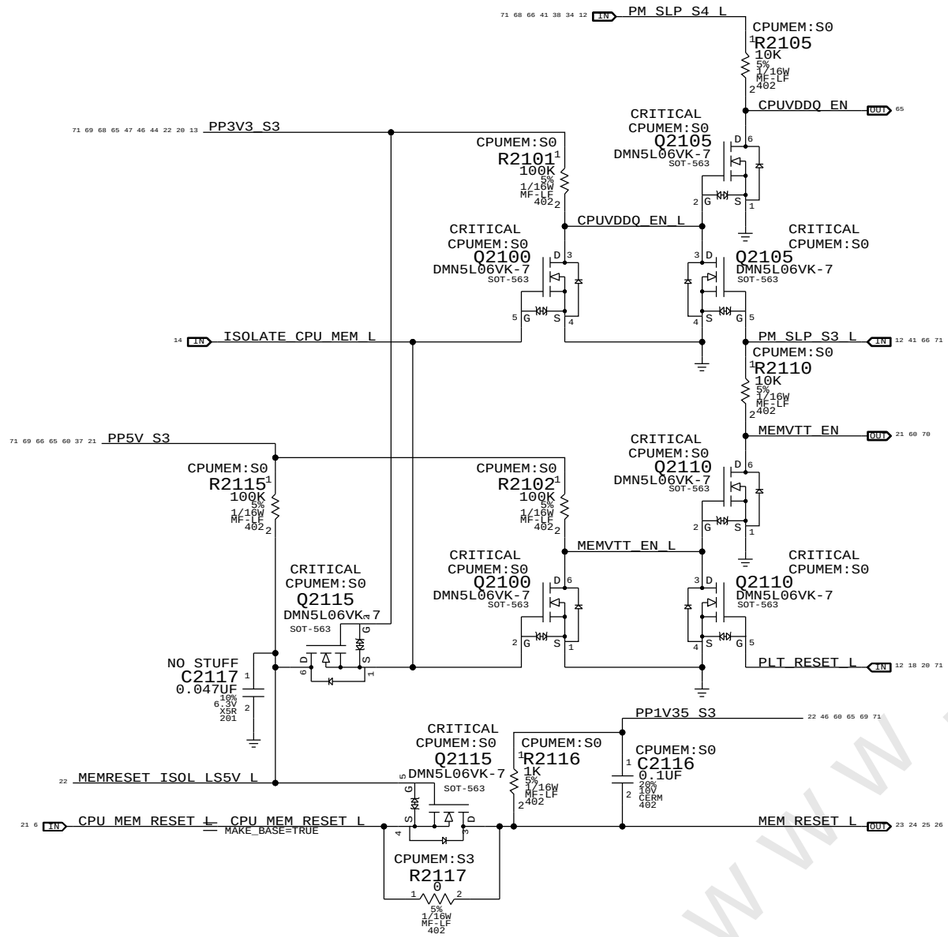
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



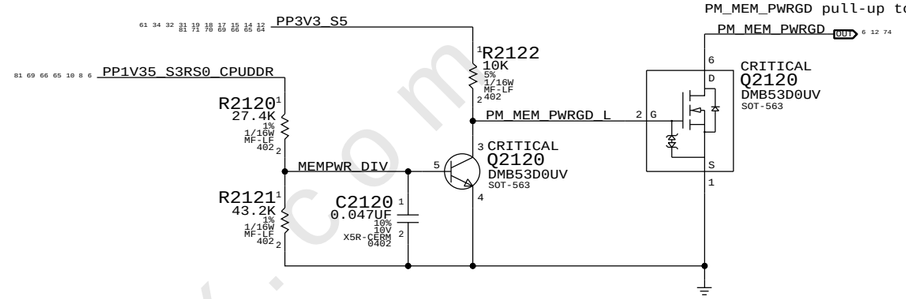
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

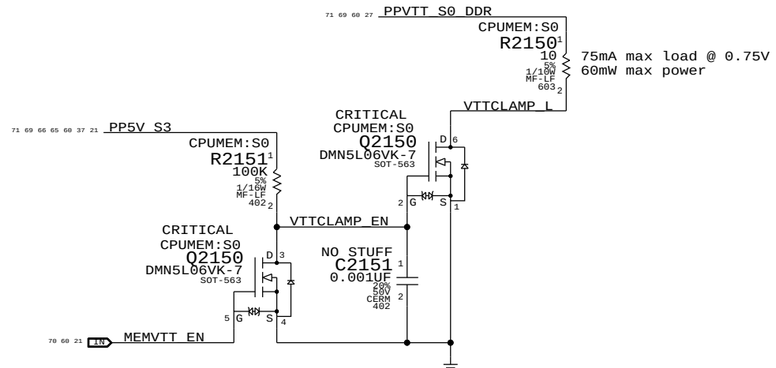
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



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PAGE TITLE: CPU Memory S3 Support

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

21 IN MEMRESET_ISOL_LS5V_L
74 7 IN CPU_DIMMA_VREFDQ
74 7 IN CPU_DIMMB_VREFDQ
7 IN CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
DDRVREF_DAC R2225 100K 5% 1/10W MF-LF 402
VREFMRGN_DQ_A_EN_RC
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC C2225 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm

CPU_MEM_VREFDQ_B_ISOL
DDRVREF_DAC R2245 100K 5% 1/10W MF-LF 402
VREFMRGN_DQ_B_EN_RC
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC C2245 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

CPU_MEM_VREFCA_A_ISOL
DDRVREF_DAC R2265 100K 5% 1/10W MF-LF 402
VREFMRGN_CA_A_EN_RC
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC C2265 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563

CPU_MEM_VREFCA_B_ISOL
DDRVREF_DAC R2285 100K 5% 1/10W MF-LF 402
VREFMRGN_CA_B_EN_RC
DDRVREF_DAC R2208 100K 5% 1/20W MF 201
DDRVREF_DAC C2285 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

PP1V35_S3 21 46 60 65 69 71

PLACE_NEAR=C2220.1:2mm
R2223 2 5% 1/20W MF 201
PLACE_NEAR=R2223.2:1mm
PP0V75_S3_MEM_VREFDQ_A 23 24 70 74 77
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
R2221 1K 1% 1/16W MF-LF 402
PLACE_NEAR=R2221.2:1mm
R2222 1K 1% 1/16W MF-LF 402
PLACE_NEAR=Q2220.6:2mm
C2220 0.022UF 10% 6.3V X5R-CERM 0201
R2220 24.9 1% 1/20W MF 201
MEM_VREFDQ_A_RC
PLACE_NEAR=C2240.1:2mm

PLACE_NEAR=C2241.1:2mm
R2241 1K 1% 1/16W MF-LF 402
PLACE_NEAR=R2243.2:1mm
PP0V75_S3_MEM_VREFDQ_B 23 26 70 74
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
R2243 2 5% 1/20W MF 201
PLACE_NEAR=R2241.2:1mm
R2242 1K 1% 1/16W MF-LF 402
PLACE_NEAR=Q2260.6:2mm
C2240 0.022UF 10% 6.3V X5R-CERM 0201
R2240 24.9 1% 1/20W MF 201
MEM_VREFDQ_B_RC
PLACE_NEAR=C2260.1:2mm

PLACE_NEAR=C2261.1:2mm
R2261 1K 1% 1/16W MF-LF 402
PLACE_NEAR=R2263.2:1mm
PP0V75_S3_MEM_VREFCA_A 23 24 70 74 77
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
R2263 2 5% 1/20W MF 201
PLACE_NEAR=R2261.2:1mm
R2262 1K 1% 1/16W MF-LF 402
PLACE_NEAR=Q2220.3:2mm
C2260 0.022UF 10% 6.3V X5R-CERM 0201
R2260 24.9 1% 1/20W MF 201
MEM_VREFCA_A_RC
PLACE_NEAR=C2280.1:2mm

PLACE_NEAR=C2281.1:2mm
R2281 1K 1% 1/16W MF-LF 402
PLACE_NEAR=R2283.2:1mm
PP0V75_S3_MEM_VREFCA_B 25 26 70 74
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
R2283 2 5% 1/20W MF 201
PLACE_NEAR=R2281.2:1mm
R2282 1K 1% 1/16W MF-LF 402
PLACE_NEAR=Q2260.3:2mm
C2280 0.022UF 10% 6.3V X5R-CERM 0201
R2280 24.9 1% 1/20W MF 201
MEM_VREFCA_B_RC

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

47 46 44 22 71 20 18 13 PP3V3_S3
OMIT R2218 SHORT NONE NONE NONE NONE 402
PP3V3_S3_VREFMRGN MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC

44 22 18 13 76 71 68 63 IN SMBUS_PCH_CLK
44 22 18 13 76 71 68 63 BI SMBUS_PCH_DATA
Addr=0x98(WR)/0x99(RD)

U2200 MSOP DAC55774
VDD 8
SCL 6 SDA 7 A0 9 A1 10 GND 3
VOUTA 1 VOUTB 2 VOUTC 4 VOUTD 5
VREFMRGN_DQ_A
VREFMRGN_DQ_B
VREFMRGN_CA_AB
VREFMRGN_MEMVREG_FBVREF

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC

U2201 PCA9557 QFN
VCC 16
Addr=0x30(WR)/0x31(RD)
A0 3 A1 4 A2 5
(OD) P0 6 NC
P1 7 VREFMRGN_DQ_A_EN
P2 9 VREFMRGN_DQ_B_EN
P3 10 VREFMRGN_CA_A_EN
P4 11 VREFMRGN_CA_B_EN
P5 12 VREFMRGN_MEMVREG_EN
P6 13 VREFMRGN_FRAMEBUF_EN
P7 14 NC
RESET* 15
THRM PAD 17 GND 8

76 71 68 63 44 22 18 13 IN SMBUS_PCH_CLK
76 71 68 63 44 22 18 13 BI SMBUS_PCH_DATA

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

20 IN PCA9557D_RESET_L

PP3V3_S3 13 20 21 22 44 46 47 65 68 69 71
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402
DDRREG_FB OUT 60

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF
DDRVREF_DAC R2217 1M 5% 1/10W MF-LF 402

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2215 100K 5% 1/20W MF 201

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

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PAGE TITLE: DDR3 VREF MARGINING
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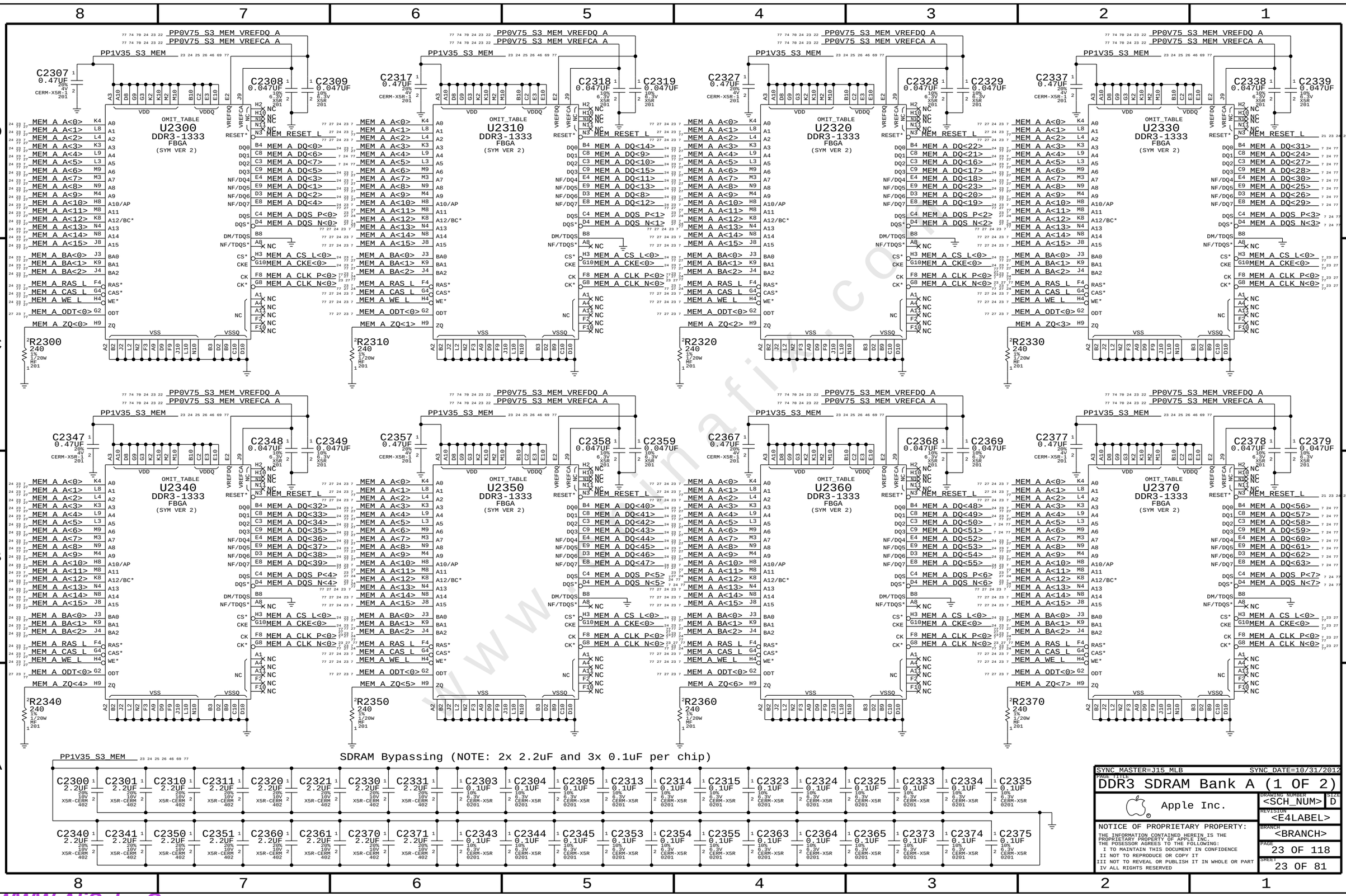

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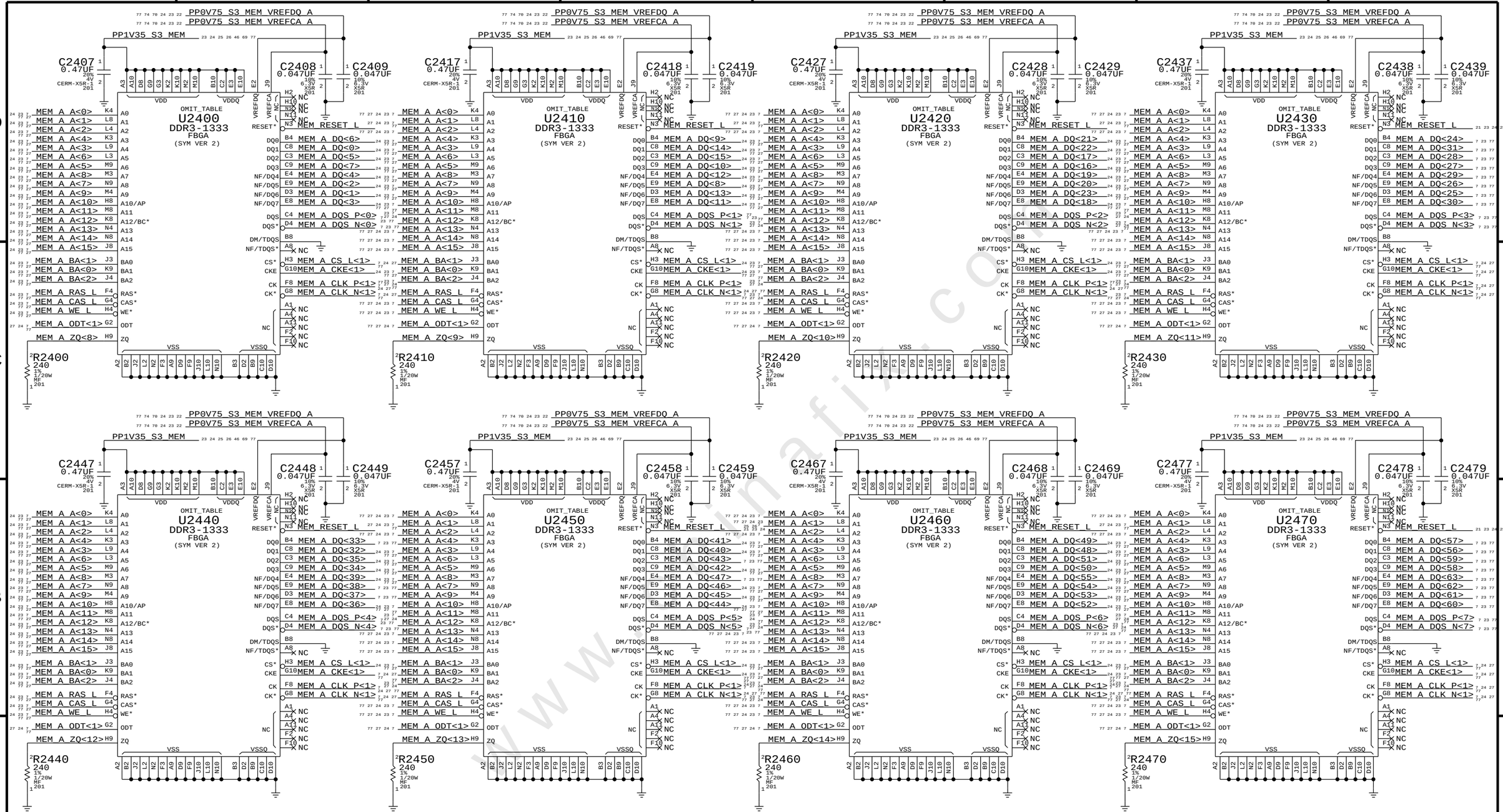

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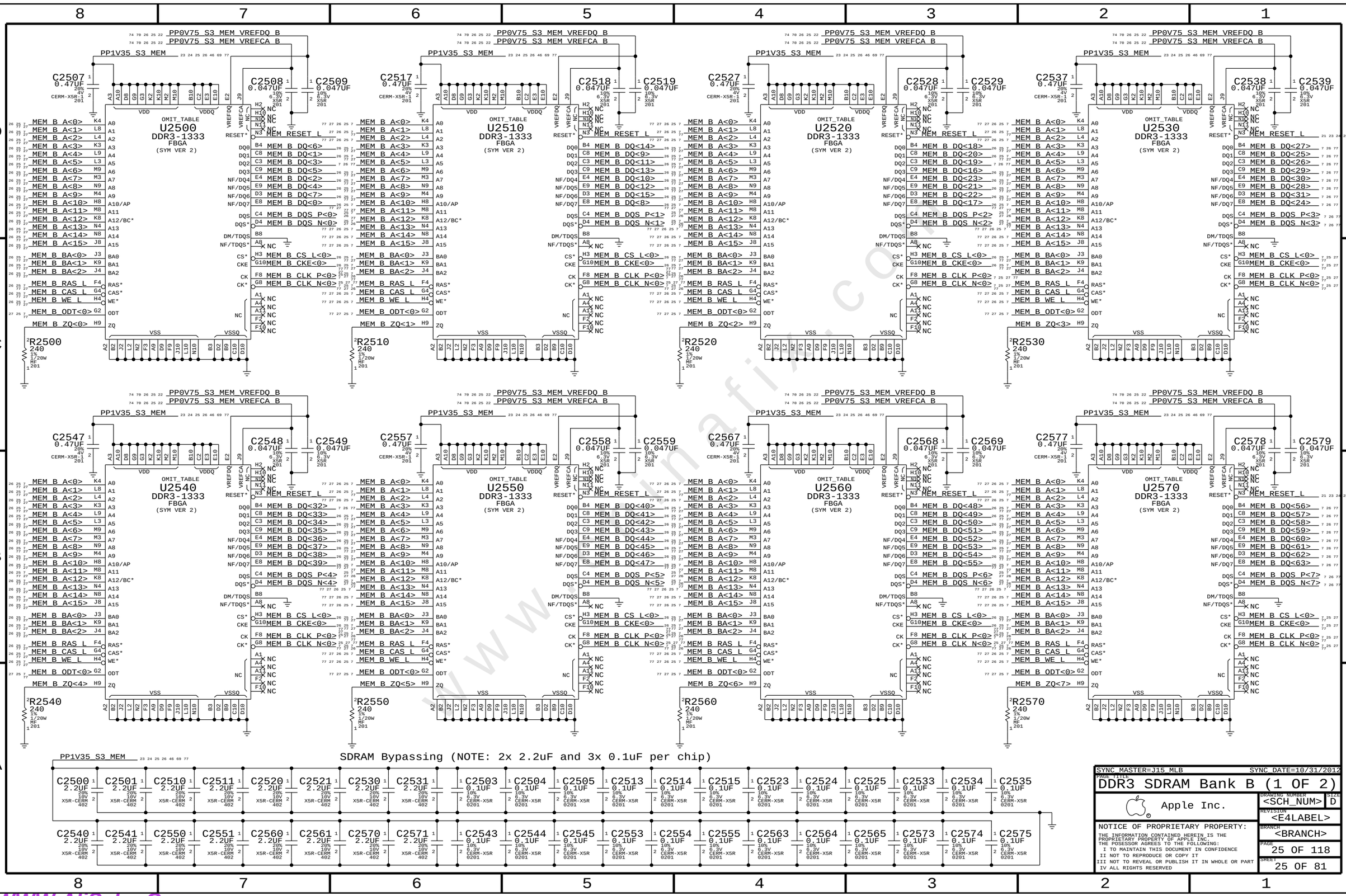

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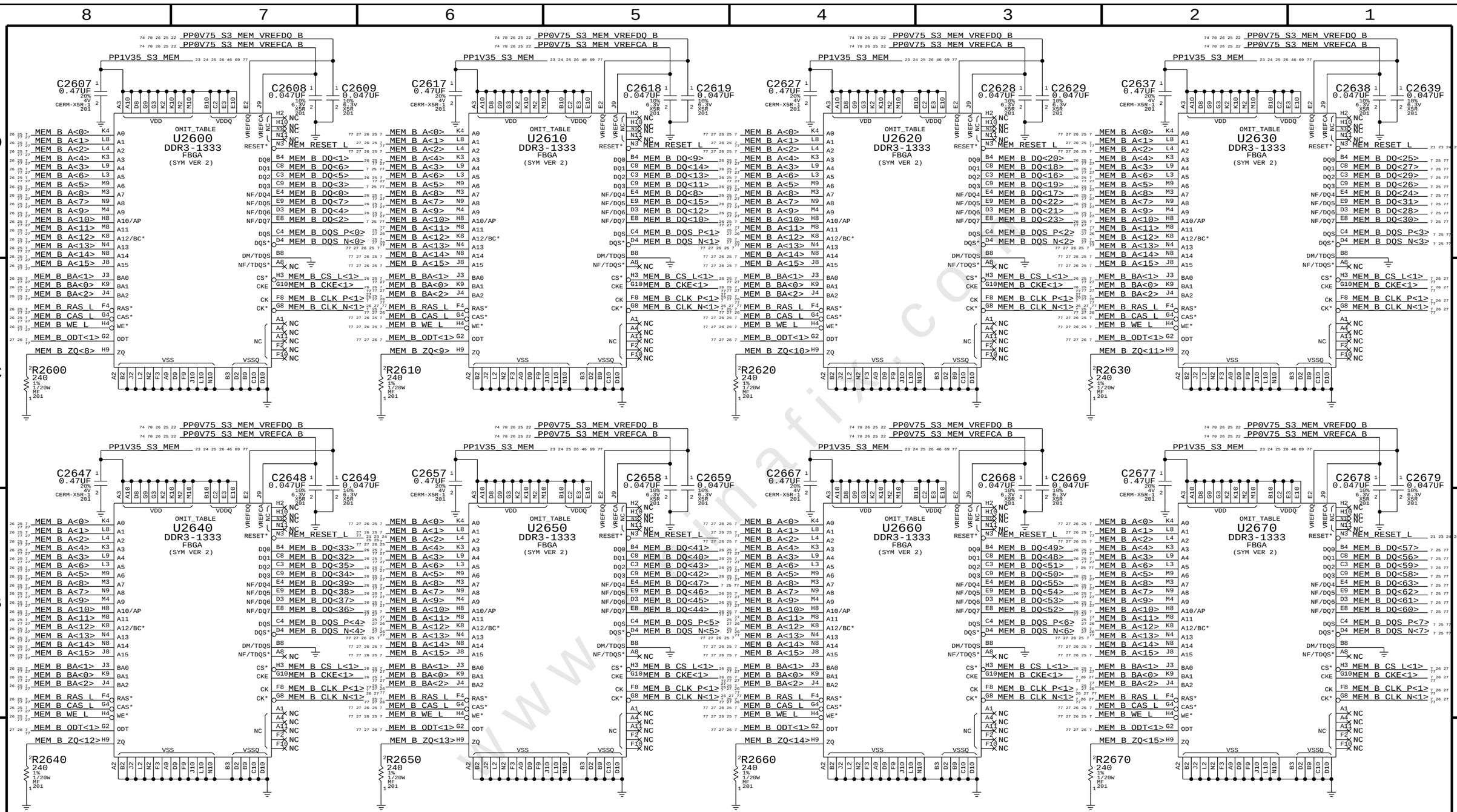

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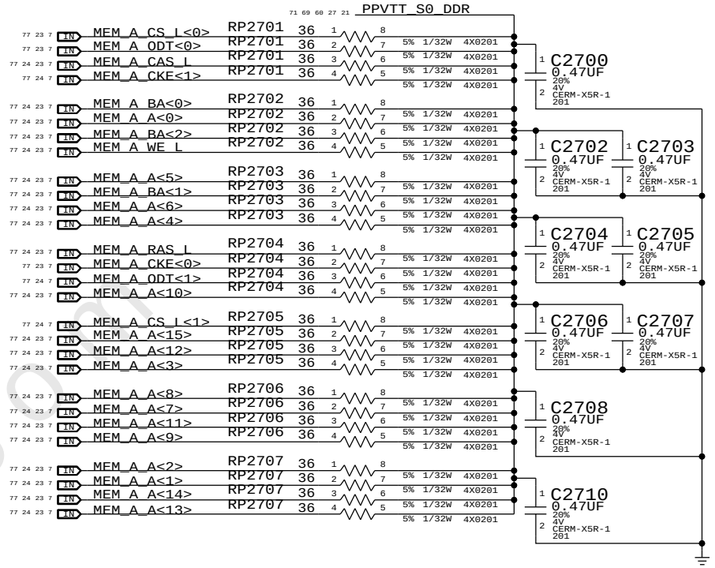
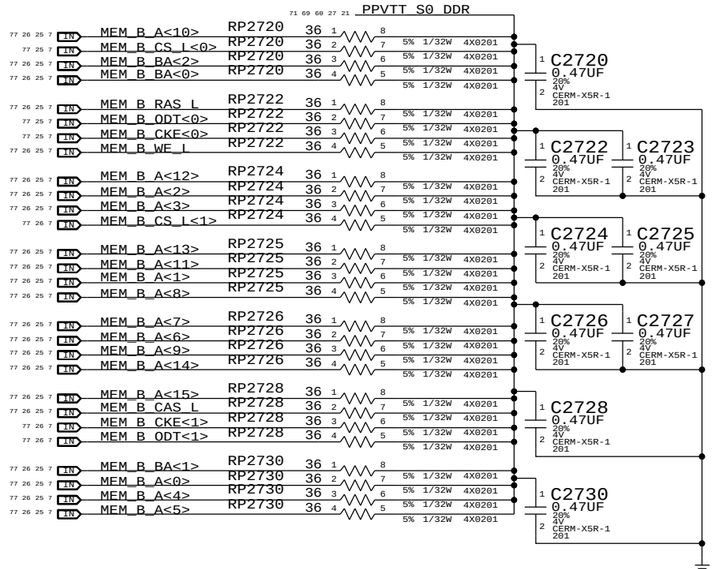
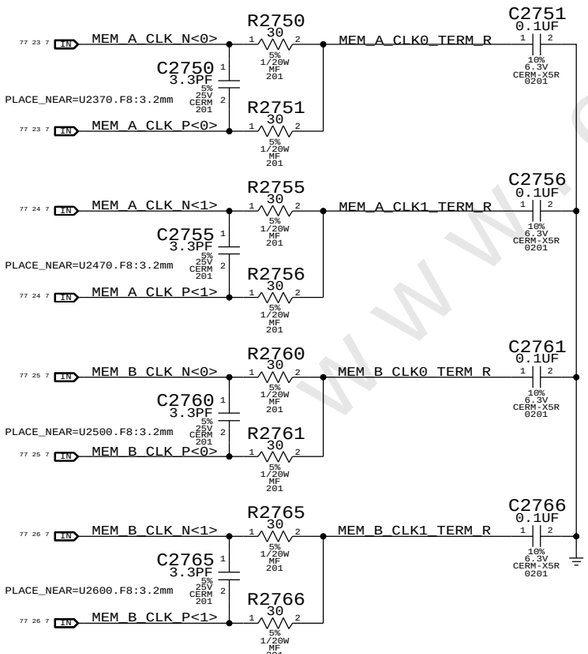
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



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CRITICAL
OMIT_TABLE

U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)

PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9 PERP_0
PCIE_TBT_R2D_C_N<0>	C2801 0.1UF	PCIE_TBT_R2D_N<0>	AA10 PERN_0
PCIE_TBT_R2D_C_P<1>	C2802 0.1UF	PCIE_TBT_R2D_P<1>	AA12 PERP_1
PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13 PERN_1
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15 PERP_2
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16 PERN_2
PCIE_TBT_R2D_C_P<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18 PERP_3
PCIE_TBT_R2D_C_N<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19 PERN_3

PETP_0	AD5	PCIE_TBT_D2R_C_P<0> → C2840 0.1UF → PCIE_TBT_D2R_P<0> OUT
PETN_0	AD7	PCIE_TBT_D2R_C_N<0> → C2841 0.1UF → PCIE_TBT_D2R_N<0> OUT
PETP_1	AD9	PCIE_TBT_D2R_C_P<1> → C2842 0.1UF → PCIE_TBT_D2R_P<1> OUT
PETN_1	AD11	PCIE_TBT_D2R_C_N<1> → C2843 0.1UF → PCIE_TBT_D2R_N<1> OUT
PETP_2	AD13	PCIE_TBT_D2R_C_P<2> → C2844 0.1UF → PCIE_TBT_D2R_P<2> OUT
PETN_2	AD15	PCIE_TBT_D2R_C_N<2> → C2845 0.1UF → PCIE_TBT_D2R_N<2> OUT
PETP_3	AD17	PCIE_TBT_D2R_C_P<3> → C2846 0.1UF → PCIE_TBT_D2R_P<3> OUT
PETN_3	AD19	PCIE_TBT_D2R_C_N<3> → C2847 0.1UF → PCIE_TBT_D2R_N<3> OUT

MISC

- TBT_PCIE_RESET_L — P5 PERST_OD_N
- TBT_PWR_ON_POC_RST_L — R4 PWR_ON_POC_RSTN
- RSENSE U20 TBT_RSENSE
- RBIAS W20 TBT_RBIAS — R2855 1K 1% 1/20W MF 201 → PP3V3_TBTLC
- RSVD AD1, L8
- TP_TBT_MONDC0 — AD23 MONDC0
- TP_TBT_MONDC1 — AC24 MONDC1
- DEBUG: For monitoring current/voltage
  - TBT_MONOBSP — W18 MONOBSP
  - TBT_MONOBSN — W16 MONOBSN
- DEBUG: For monitoring clock
  - TBT_THERMD_P — AB7 THERMDA
  - Use AA8 GND ball for THERM_DN
- TBT_SPI_MOSI — AA2 EE_DI
- TBT_SPI_MISO — Y3 EE_DO
- TBT_SPI_CS_L — T5 EE_CS_N
- TBT_SPI_CLK — U8 EE_CLK
- JTAG_TBT_TDI — W2 TDI
- JTAG_TBT_TMS — AB1 TMS
- JTAG_TBT_TCK — AA6 TCK
- JTAG_TBT_TDO — U6 TDO
- TBT_TEST_EN — R6 TEST_EN
- TBT_TEST_PWR_GOOD — W8 TEST_PWR_GOOD

Used for straps in host mode

PCIE_RST_0_N	W6	TP_TBT_PCIE_RESET0_L
PCIE_RST_1_N	AB3	TBT_DFT_STRAP_1
PCIE_RST_2_N	AD3	TBT_ROM_SECURITY_XOR
PCIE_RST_3_N	V1	TBT_DFT_STRAP_3
PCIE_CLKREQ_OD_N	V3	TBT_CLKREQ_L OUT 11
REFCLK_100_IN_P	AB21	PCIE_CLK100M_TBT_P IN 11 76
REFCLK_100_IN_N	AD21	PCIE_CLK100M_TBT_N IN 11 76
XTAL_25_IN	AA24	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	AB23	NC_TBT_XTAL25OUT 72
TMU_CLK_OUT	AA4	TBT_TMU_CLK_OUT

DISPLAY PORTS

DPSRC_3_P	A14	NC_DP_TBTSRC_ML_CP<3> 72
DPSRC_3_N	B15	NC_DP_TBTSRC_ML_CN<3> 72
DPSRC_2_P	A12	NC_DP_TBTSRC_ML_CP<2> 72
DPSRC_2_N	B13	NC_DP_TBTSRC_ML_CN<2> 72
DPSRC_1_P	A10	NC_DP_TBTSRC_ML_CP<1> 72
DPSRC_1_N	B11	NC_DP_TBTSRC_ML_CN<1> 72
DPSRC_0_P	A8	NC_DP_TBTSRC_ML_CP<0> 72
DPSRC_0_N	B9	NC_DP_TBTSRC_ML_CN<0> 72
DPSRC_AUX_P	J4	NC_DP_TBTSRC_AUXCH_CP 72
DPSRC_AUX_N	J2	NC_DP_TBTSRC_AUXCH_CN 72
DPSRC_HPD_OD	AC2	DP_TBTSRC_HPD 28

DP_TBTSNK0_ML_P<3>	E14	DPSNK0_3_P
DP_TBTSNK0_ML_N<3>	D13	DPSNK0_3_N
DP_TBTSNK0_ML_P<2>	E16	DPSNK0_2_P
DP_TBTSNK0_ML_N<2>	D15	DPSNK0_2_N
DP_TBTSNK0_ML_P<1>	E18	DPSNK0_1_P
DP_TBTSNK0_ML_N<1>	D17	DPSNK0_1_N
DP_TBTSNK0_ML_P<0>	E20	DPSNK0_0_P
DP_TBTSNK0_ML_N<0>	D19	DPSNK0_0_N
DP_TBTSNK0_AUXCH_P	G4	DPSNK0_AUX_P
DP_TBTSNK0_AUXCH_N	G2	DPSNK0_AUX_N
DP_TBTSNK0_HPD	AB5	DPSNK0_HPD
DP_TBTSNK1_ML_P<3>	E6	DPSNK1_3_P
DP_TBTSNK1_ML_N<3>	D5	DPSNK1_3_N
DP_TBTSNK1_ML_P<2>	E8	DPSNK1_2_P
DP_TBTSNK1_ML_N<2>	D7	DPSNK1_2_N
DP_TBTSNK1_ML_P<1>	E10	DPSNK1_1_P
DP_TBTSNK1_ML_N<1>	D9	DPSNK1_1_N
DP_TBTSNK1_ML_P<0>	E12	DPSNK1_0_P
DP_TBTSNK1_ML_N<0>	D11	DPSNK1_0_N
DP_TBTSNK1_AUXCH_P	H3	DPSNK1_AUX_P
DP_TBTSNK1_AUXCH_N	H1	DPSNK1_AUX_N
DP_TBTSNK1_HPD	U4	DPSNK1_HPD

TBT_A_R2D_C_P<0>	G24	PA_CIO0_TX_P/DPSRC_0_P
TBT_A_R2D_C_N<0>	E24	PA_CIO0_TX_N/DPSRC_0_N
TBT_A_D2R_P<0>	G22	PA_CIO0_RX_P
TBT_A_D2R_N<0>	E22	PA_CIO0_RX_N
TBT_A_CONFIG1_BUF	P1	PA_CONFIG1/CIO_0_LSEO
TBT_A_CONFIG2_RC	K5	PA_CONFIG2/CIO_0_LSOE
TBT_A_R2D_C_P<1>	L24	PA_CIO1_TX_P/DPSRC_2_P
TBT_A_R2D_C_N<1>	J24	PA_CIO1_TX_N/DPSRC_2_N
TBT_A_D2R_P<1>	L22	PA_CIO1_RX_P
TBT_A_D2R_N<1>	J22	PA_CIO1_RX_N
TBT_A_LSTX	N8	PA_LSTX/CIO_1_LSEO
TBT_A_LSRX	J6	PA_LSRX/CIO_1_LSOE
TBT_A_HV_EN	R8	GPIO_0/PA_HV_EN/BYP0
TBT_A_CIO_SEL	N2	GPIO_10/PA_CIO_SEL/BYP1
TBT_A_DP_PWRDN	P3	GPIO_12/PA_DP_PWRDN/BYP2

PB_CIO2_TX_P/DPSRC_0_P	R24	TBT_B_R2D_C_P<0>
PB_CIO2_TX_N/DPSRC_0_N	N24	TBT_B_R2D_C_N<0>
PB_CIO2_RX_P	R22	TBT_B_D2R_P<0>
PB_CIO2_RX_N	N22	TBT_B_D2R_N<0>
PB_CONFIG1/CIO_2_LSEO	D3	TBT_B_CONFIG1_BUF
PB_CONFIG2/CIO_2_LSOE	M1	TBT_B_CONFIG2_RC
PB_CIO3_TX_P/DPSRC_2_P	W24	TBT_B_R2D_C_P<1>
PB_CIO3_TX_N/DPSRC_2_N	U24	TBT_B_R2D_C_N<1>
PB_CIO3_RX_P	W22	TBT_B_D2R_P<1>
PB_CIO3_RX_N	U22	TBT_B_D2R_N<1>
PB_LSTX/CIO_3_LSEO	M5	TBT_B_LSTX
PB_LSRX/CIO_3_LSOE	P7	TBT_B_LSRX
PB_DPSRC_1_P	A20	DP_TBTPB_ML_C_P<1>
PB_DPSRC_1_N	B21	DP_TBTPB_ML_C_N<1>
PB_DPSRC_3_P	A22	DP_TBTPB_ML_C_P<3>
PB_DPSRC_3_N	B23	DP_TBTPB_ML_C_N<3>
PB_AUX_P	K3	DP_TBTPB_AUXCH_C_P
PB_AUX_N	K1	DP_TBTPB_AUXCH_C_N
PB_DPSRC_HPD	N6	DP_TBTPB_HPD
GPIO_1/PB_HV_EN/BYP0	F1	TBT_B_HV_EN
GPIO_11/PB_CIO_SEL/BYP1	R2	TBT_B_CIO_SEL
GPIO_13/PB_DP_PWRDN/BYP2	F3	TBT_B_DP_PWRDN

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

GPIO_2/TMU_CLK_IN/AC_PRESENT

- GPIO_3/FORCE_PWR — L6 TBT_PWR_EN IN 20
- GPIO_4/WAKE_OD_N — H5 SMC_PME_S4_DARK_L OUT 20 41 42 43
- GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD — Y7 TBT_CIO_PLUG_EVENT_L OUT 14 20
- GPIO_6_OD/CIO_SDA_OD — Y1 HDMITBTMUX_SEL_TBT IN 28 70
- GPIO_7_OD/CIO_SCL_OD — T7 TBT_GPIO7
- GPIO_8/EN_CIO_PWR_OD* — V7 TBT_EN_CIO_PWR_L OUT 28 29
- GPIO_9/SX_CTRL_OD* — M7 TBT_BATLOW_L IN 28 30
- GPIO_14 — T1 TBTDP_AUXIO_EN OUT 28 31 32
- GPIO_15 — T3 TBT_DDC_XBAR_EN_L OUT 28 33

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF	DP_TBTSNK1_AUXCH_N

All caps: 16V X5R-CERM 0201 10%

Power / straps

- PP3V3_TBTLC → R2890 3.3K, R2891 3.3K, C2890 1UF 10V 6-10V CERM 402 (BYPASS=U2890:2mm), R2892 3.3K, R2893 3.3K
- CRITICAL OMIT_TABLE
- U2890 4MBIT W25X40CLXIG USON
  - (TBT_SPI_MOSI) 5 DI/IO0
  - (TBT_SPI_CLK) 6 CLK
  - (TBT_SPI_CS_L) 1 CS*
  - TBTROM_WP_L 3 WP*
  - TBTROM_HOLD_L 7 HOLD*
  - DO/IO1 2 (TBT_SPI_MISO)
  - VCC 8
  - GND THRM_PAD 4 9
- OMIT R2815 NOSTUFF
- R2829 10K
- R2825 100
- R2830 100K → DP_TBTSNK0_HPD
- R2831 100K → TBT_A_HPD
- R2855 1K → PP3V3_TBTLC

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.

If strap != bit then security is enabled?

- NO STUFF R2867 10K → PP3V3_TBTLC
- R2861 10K, R2862 10K, R2863 10K → PP3V3_TBTLC

Divides 3.3V to 1.8V

- R2895 806 → SYSCLK_CLK25M_TBT
- NO STUFF R2899 10K
- R2896 1K → PP3V3_TBTLC
- R2881 100K → TBT_EN_CIO_PWR_L
- R2880 100K → TBT_DDC_XBAR_EN_L
- R2882 100K → HDMITBTMUX_SEL_TBT
- R2878 100K → TBTDP_AUXIO_EN
- R2879 100K → DP_TBTSRC_HPD
- R2884 100K → TBT_BATLOW_L
- NO STUFF R2885 10K → TBT_A_DP_PWRDN
- NO STUFF R2886 10K → TBT_B_DP_PWRDN
- R2888 10K → TBT_A_HV_EN
- R2887 10K → TBT_B_HV_EN
- R2832 100K, R2883 100K → PP3V3_TBTLC
- R2884 100K → PP3V3_S4_TBT

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

PAGE TITLE: Thunderbolt Host (1 of 2)

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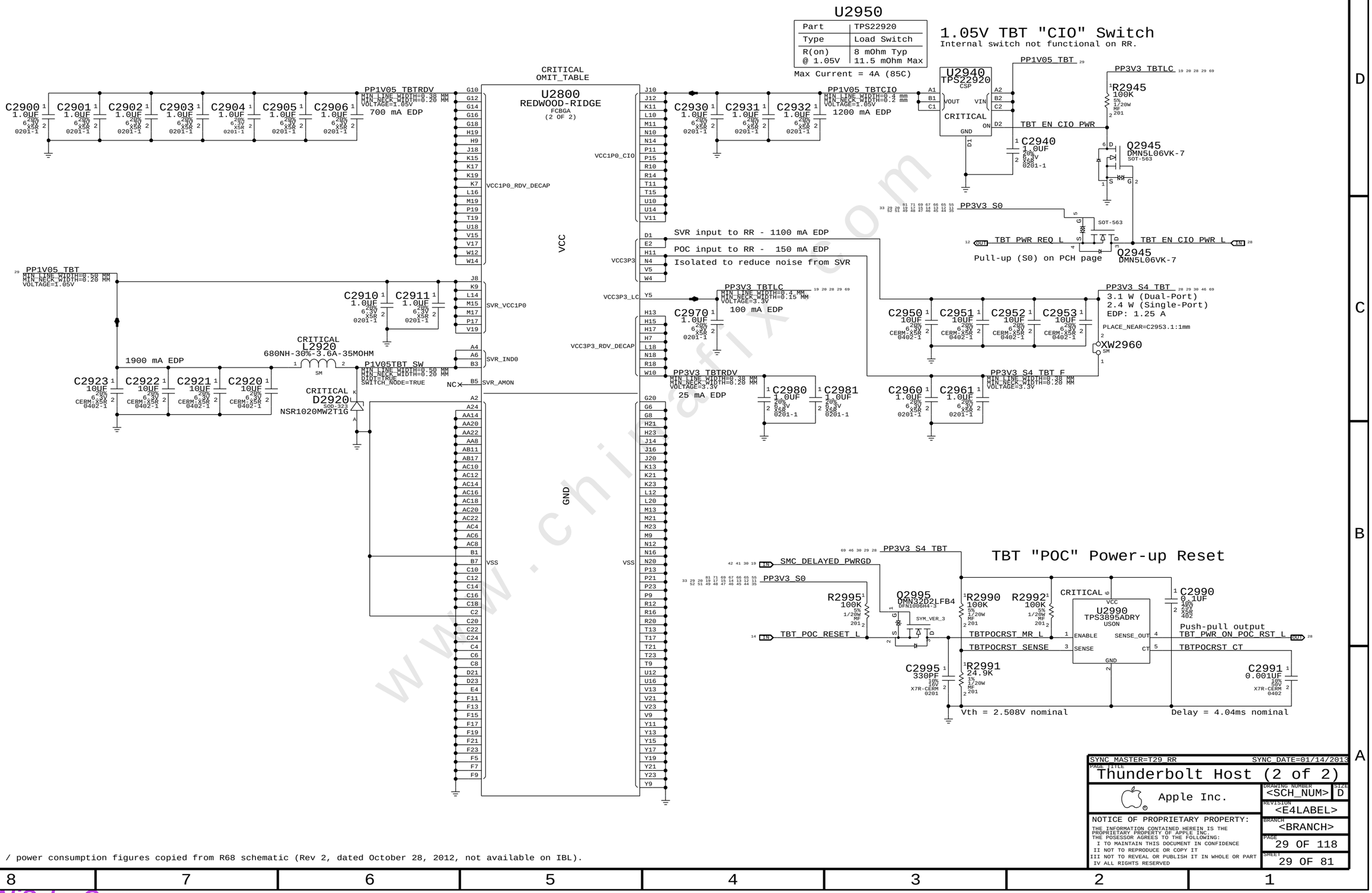

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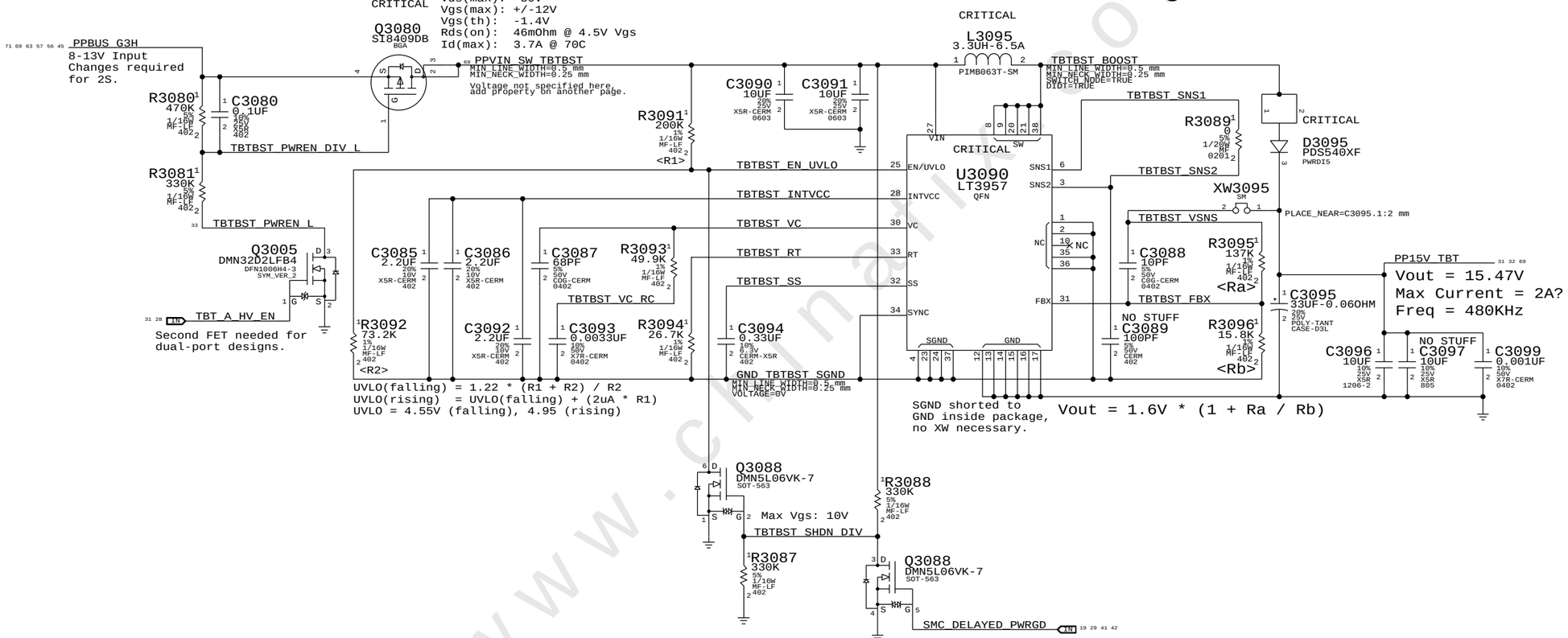
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

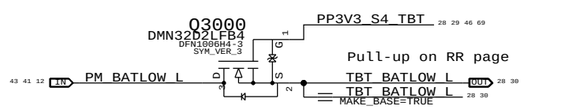
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



BATLOW# Isolation



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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

PP3V3_S5

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 0603
C3281 0.1UF 10% 16V X5R-CERM 0201

PP15V_TBT 15.75V Max

C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 25V X5R 402

CRITICAL U3210 CD3211A0RGPR QFN
V3P3 V3P3OUT VHV OUT ENHVU FAULTZ EN ISET_V3P3 HV_EN ISET_S0 S0 ISET_S3 GND THRM PAD

C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V X5R 402

PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP3V3RHV_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_R_L

TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3

TBTHV:P15V
12V: See below
R3210 22.6K 1% 1/20W MF 2012
TBTHV:P15V
R3211 22.6K 1% 1/20W MF 2012
R3212 36.5K 1% 1/20W MF 2012
<RV3P3>

TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R

TBTHV:P15V
R3213 22.6K 1% 1/20W MF 2012
<RHVS3>
TBTHV:P15V
R3214 22.6K 1% 1/20W MF 2012
<RHVS0>

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X7R-CERM 0402
R3201 12 5% 1/10W MF 201

TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

TBT Dir DP Dir

TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
C3274 0.47UF 20% 4V_201 CERM-X5R-1
C3275 0.47UF 20% 4V_201 CERM-X5R-1
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>

GND_VOID=TRUE (Both C's)
R3294 1K 5% 1/20W MF 201
R3295 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE

TBT: RX_0

DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>

R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201

TBT: Unused

TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N

TBT: RX_1

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201

C3202 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL
SHIELD PINS
J3200 MDP-J44 F-RT-TH
PORT B
SHIELD PINS
514-0876

B2	HPD	GND0	B1
B4	CONFIG1	ML_LANE0P	B3
B6	CONFIG2	ML_LANE0N	B5
B8	GND2	GND1	B7
B10	ML_LANE3P	ML_LANE1P	B9
B12	ML_LANE3N	ML_LANE1N	B11
B14	GND4	GND3	B13
B16	AUX_CHP	ML_LANE2P	B15
B18	AUX_CHN	ML_LANE2N	B17
B20	DP_PWR	RETURN	B19

TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3205 0.01UF 10% 25V X5R-CERM 0201

TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3206 0.01UF 10% 25V X5R-CERM 0201

DP Dir TBT Dir
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0

TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1

GND_VOID=TRUE (Both C's)
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201

DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201

CRITICAL U3220 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
VDD GND_THMPAD

GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V_201 CERM-X5R-1
C3276 0.47UF 20% 4V_201 CERM-X5R-1
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201

TBT_A_D2R_N<1>	TB-	TB_ENA	TBT_A_CIO_SEL
TBT_A_D2R_P<1>	TB+	AUXIO_EN	TBTDP_AUXIO_EN
		DP_PD	TBT_A_DP_PWRDN
	AUX-	(IPU)AUXIO-	TBT_A_D2R1_AUXDDC_N
	AUX+	(IPD)AUXIO+	TBT_A_D2R1_AUXDDC_P
DP_TBTPA_AUXCH_C_N	AUX+		
DP_TBTPA_AUXCH_C_P			
DP_TBTPA_DDC_DATA	DDC_DAT		
DP_TBTPA_DDC_CLK	DDC_CLK		
TBT_A_CONFIG1_BUF	CA_DETOUT	CA_DET	TBT_A_CONFIG1_RC
DP_TBTPA_ML_C_P<1>	DP+		
DP_TBTPA_ML_C_N<1>	DP-		
		DPML0+	DP_A_LSX_ML_P<1>
		DPML0-	DP_A_LSX_ML_N<1>
TBT_A_LSTX	LSTX (IPU)		
TBT_A_LSRX	LSRX (IPD)		
DP_TBTPA_HPD	HPDOUT	HPD	TBT_A_HPD

TBT: RX_1
TBT: LSX_A_R2P/P2R (P/N)

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT
15.75V Max
CRITICAL C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3380 22UF 20% 6.3V X5R-CERM 603
C3381 0.1UF 10% 16V X5R-CERM 0201
C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 16V X5R 402
CRITICAL U3310 CD3211A0RGPR QFN
V3P3 V3P3OUT VHV OUT ENHVU FAULTZ EN ISET_V3P3 HV_EN ISET_S0 S0 ISET_S3 GND THRM PAD
C3385 0.1UF 10% 16V X5R-CERM 0201
C3386 10UF 20% 6.3V CERM-X5R 0402
C3311 0.1UF 10% 25V 402
PP3V3_S4_TBTBPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)
PP3V3RHV_S4_TBTBPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
S4_PWR_EN
TBT_B_HV_EN
PM_SLP_S3_R_L
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
12V: See below
TBTHV:P15V R3310 22.6K 1% 1/20W MF 201
TBTHV:P15V R3311 22.6K 1% 1/20W MF 201
R3312 36.5K 1% 1/20W MF 201 <RV3P3>
TBTHV:P15V R3313 22.6K 1% 1/20W MF 201 <RHVS3>
TBTHV:P15V R3314 22.6K 1% 1/20W MF 201 <RHVS0> ILIM = 40000 / RISET
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

PP3V3_S4_TBTBPWR
C3320 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3320 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
TB- TB+ AUX- AUX+ DDC_DAT DDC_CLK CA_DETOUT DP+ DP- LSTX (IPU) LSRX (IPD) HPDOUT
TB_ENA AUXIO_EN DP_PD (IPU)AUXIO- (IPD)AUXIO+ CA_DET DPML0+ DPML0- HPD GND THMPAD
TBT_B_CIO_SEL
TBTDP_AUXIO_EN
TBT_B_DP_PWRDN
TBT_B_D2R1_AUXDDC_N
TBT_B_D2R1_AUXDDC_P
TBT: RX_1
TBT_B_CONFIG1_RC
TBT_B_HPD
TBT_B_D2R_C_N<1>
TBT_B_D2R_C_P<1>
TBT_B_D2R_N<1>
TBT_B_D2R_P<1>
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
DP_TBTPB_AUXCH_N
DP_TBTPB_AUXCH_P
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_HPD
GND_VOID=TRUE (Both C's)
C3377 0.47UF 20% 4V 201 CERM-X5R-1
C3376 0.47UF 20% 4V 201 CERM-X5R-1
C3330 0.1UF 10% 16V X5R-CERM 0201
C3331 0.1UF 10% 16V X5R-CERM 0201
C3332 0.22UF 20% 6.3V X5R 0201
C3333 0.22UF 20% 6.3V X5R 0201

L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
C3300 0.01UF 10% 50V X7R-CERM 0402
R3301 12 5% 1/20W MF 201
TBTBCONN_20_RC (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V)
C3301 0.01UF 10% 50V X7R-CERM 0402
TBTBCONN_1_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)
C3305 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_7_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)
C3306 0.01UF 10% 25V X5R-CERM 0201
(0-18.9V)
GND_VOID=TRUE

CRITICAL J3200 MDP-J44 F-RT-TH
SHIELD PINS S5 S4 S3 S2 S1
PORT A
SHIELD PINS S23 S11 S10 S9 S8 S7 S6
514-0876
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN

TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1
TBT: TX_0
TBT: TX_1
TBT: LSX_R2P/P2R (P/N)
DP Dir TBT Dir

TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>

C3374 0.47UF 20% 4V 201 CERM-X5R-1
C3375 0.47UF 20% 4V 201 CERM-X5R-1
C3378 0.22UF 20% 6.3V X5R 0201
C3379 0.22UF 20% 6.3V X5R 0201
C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.

R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201
C3302 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: Thunderbolt Connector B

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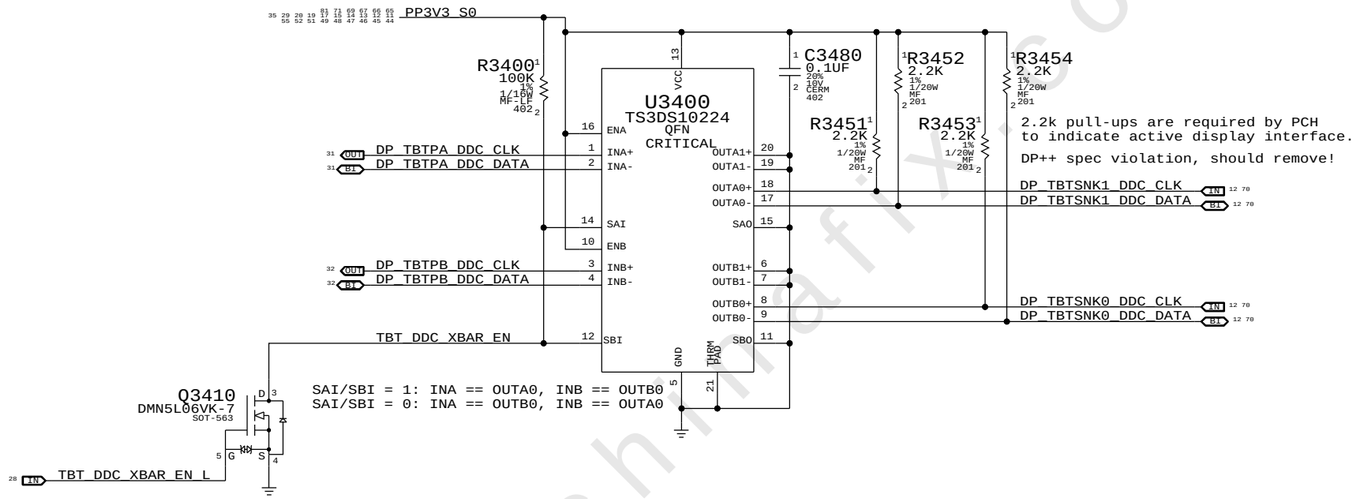
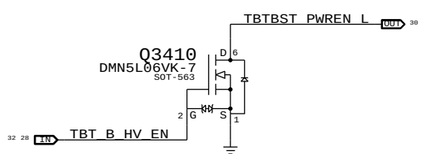
DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



SYNC_MASTER=J15_REFERENCE	SYNC_DATE=11/16/2012
PAGE TITLE	DDC Crossbar
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

AIRPORT

BLUETOOTH

Supervisor & CLKREQ # Isolation

Delay = 130 ms +/- 20%

SIGNAL_MODEL=MOJO_MUX_USBONLY

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: X29C CONNECTOR

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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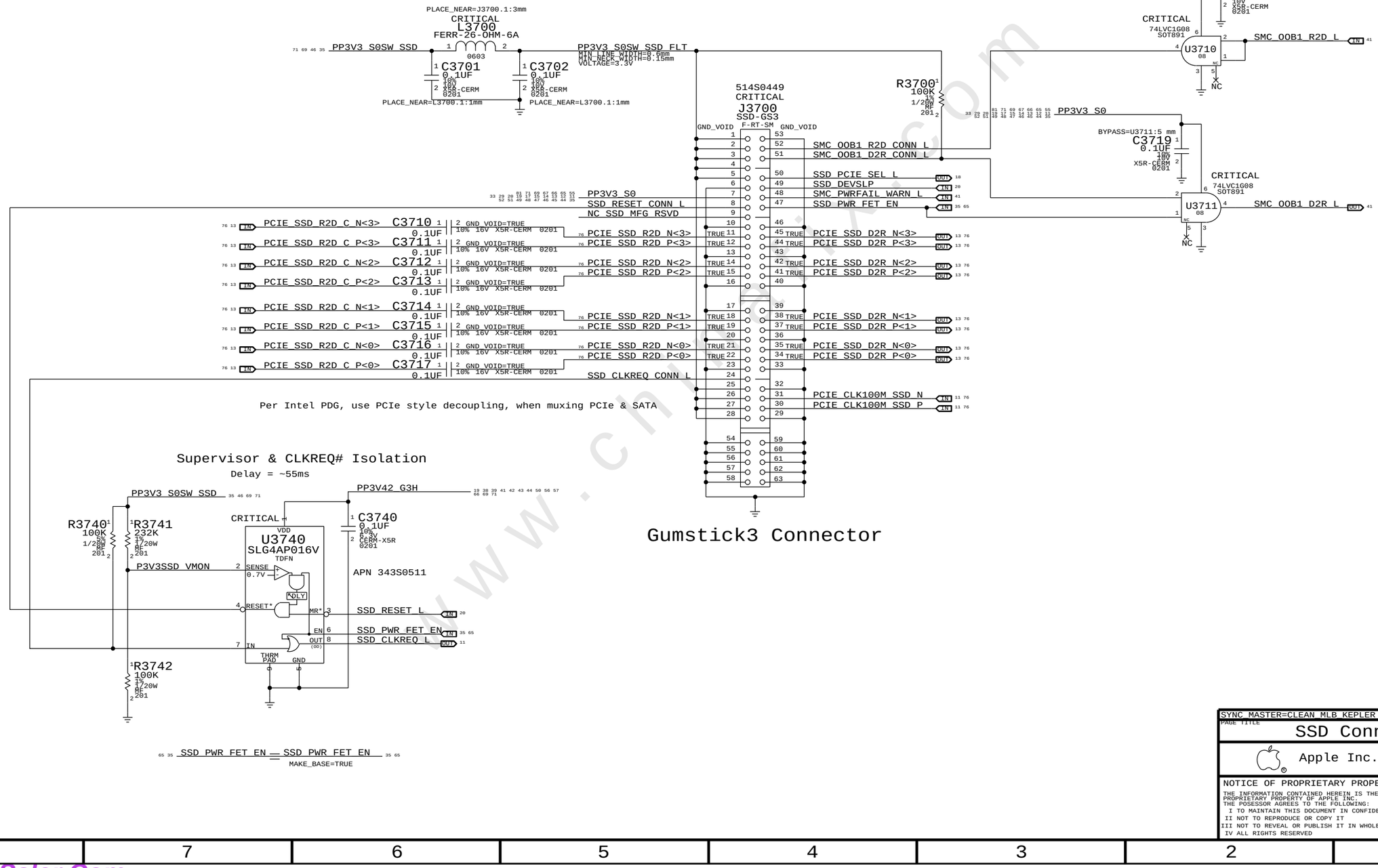

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SYNC_MASTER=CLEAN_MLB_KEPLER	SYNC_DATE=06/08/2013
PAGE TITLE	SSD Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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	BRANCH <BRANCH>
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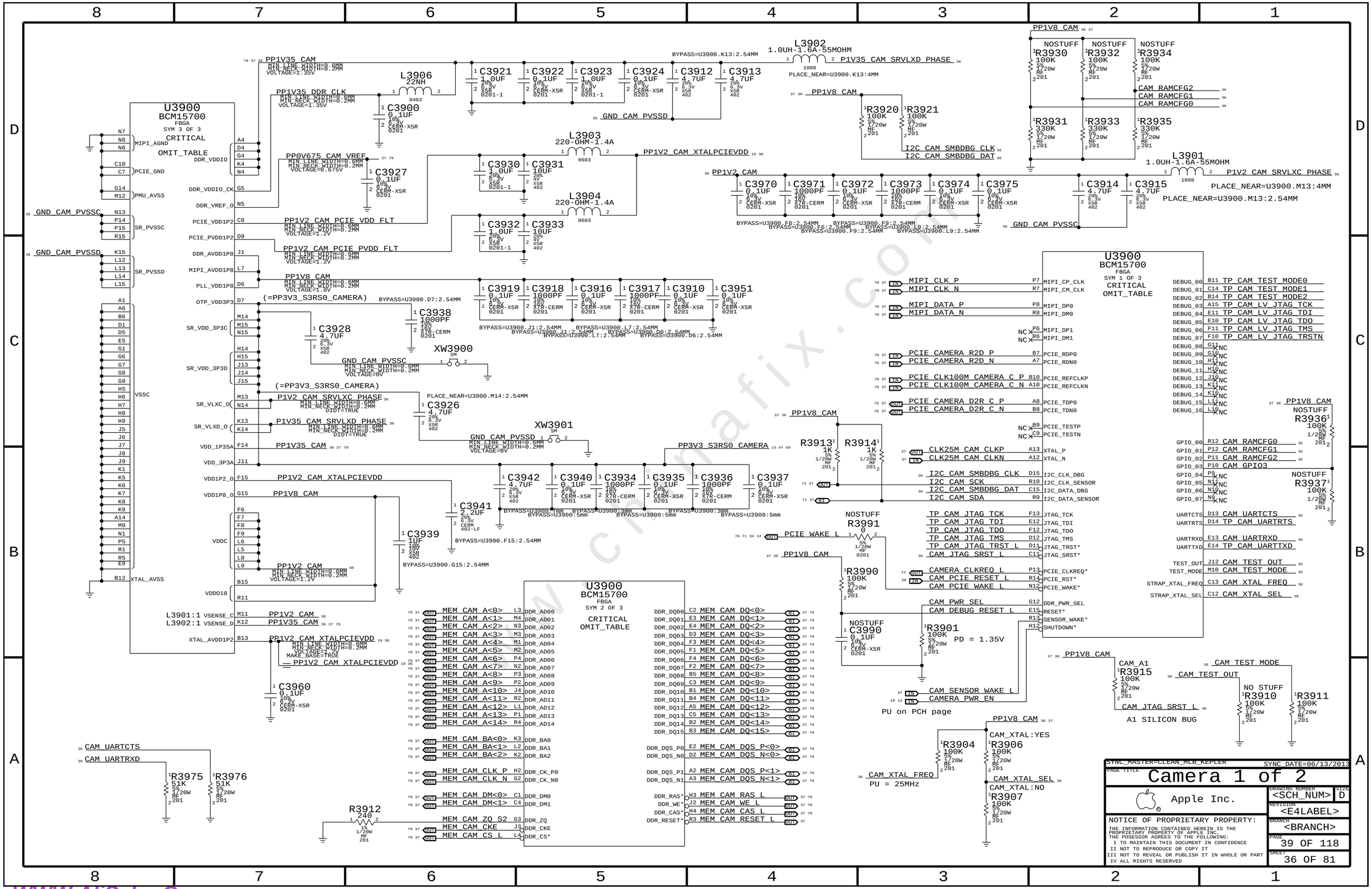

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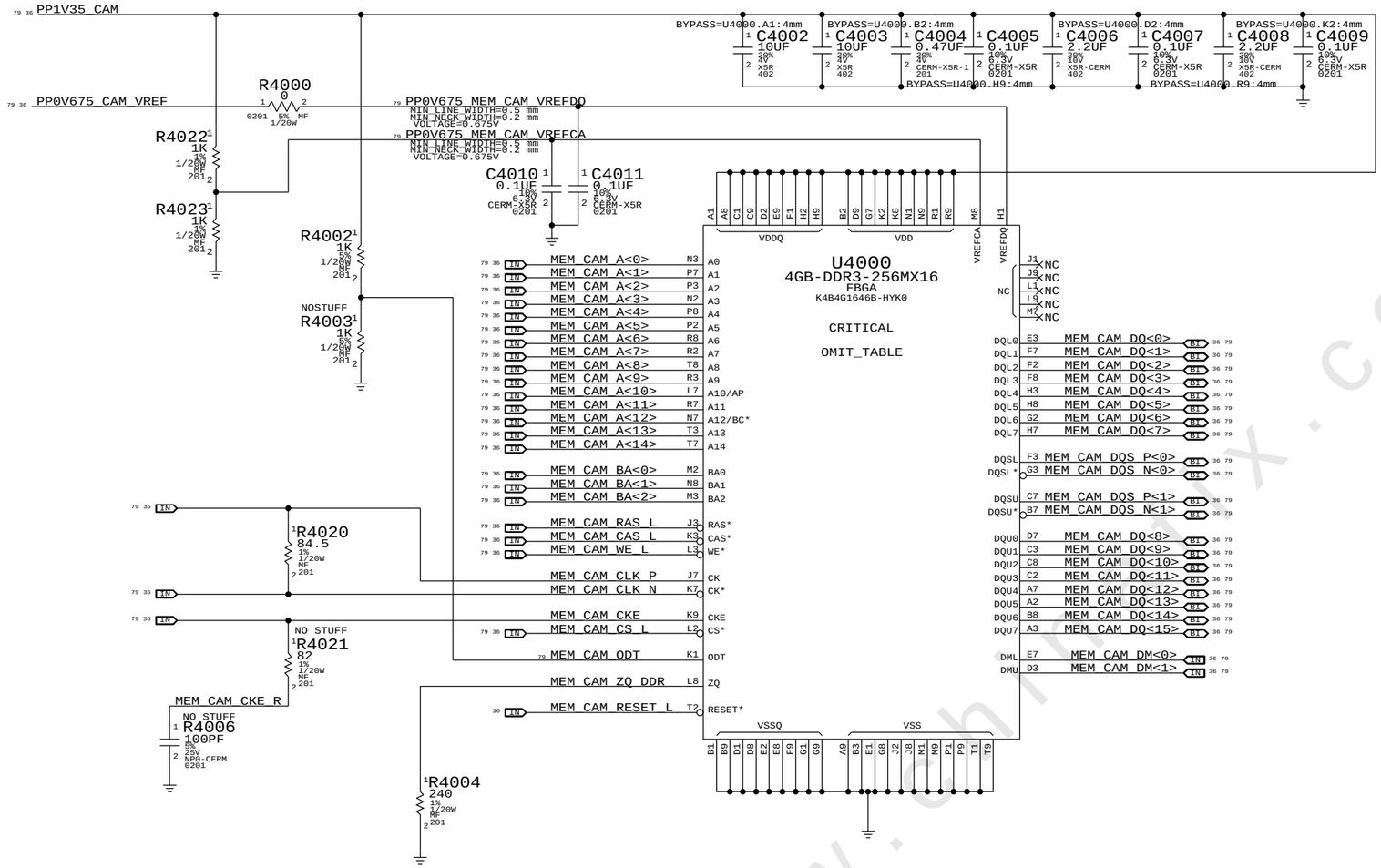

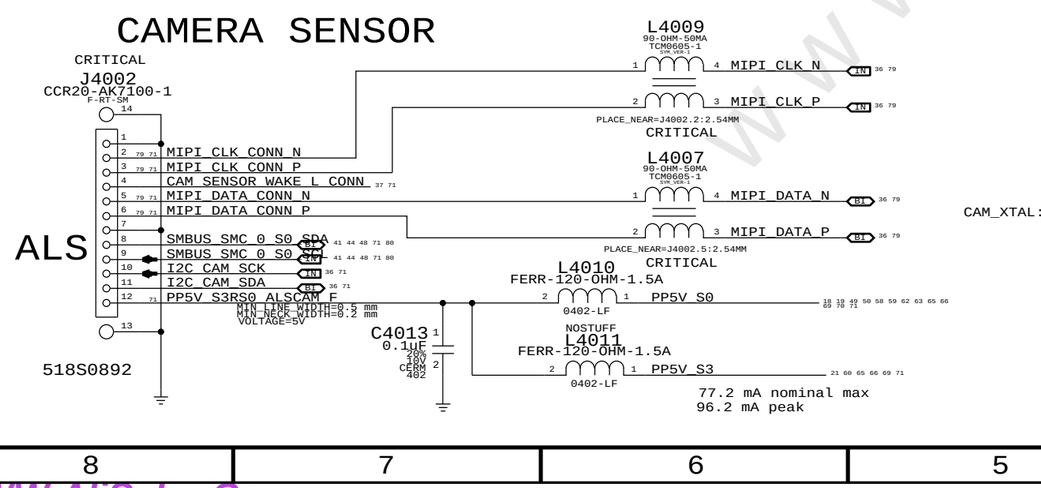

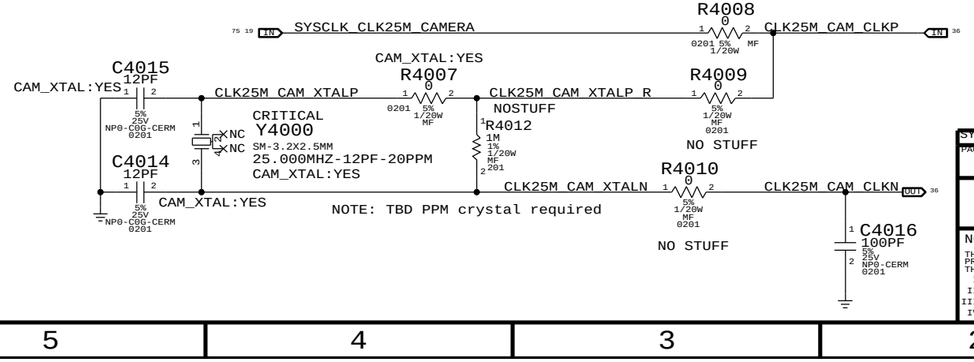

remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

SYNC_MASTER=CLEAN_MLB_KEPLER
SYNC_DATE=06/13/2013
PAGE TITLE
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Apple Inc.
DRAWING NUMBER <SCH_NUM>
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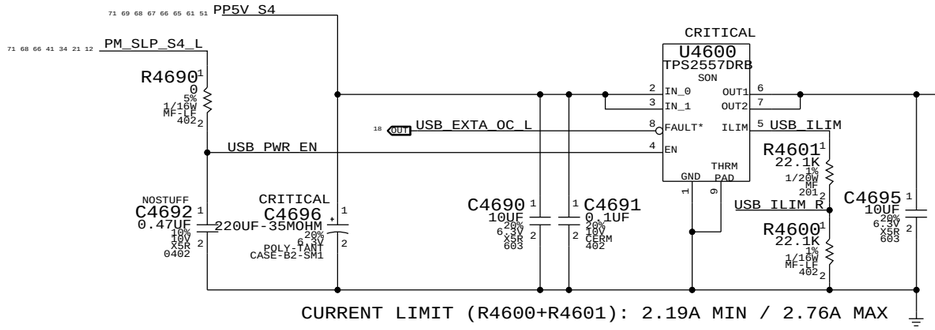
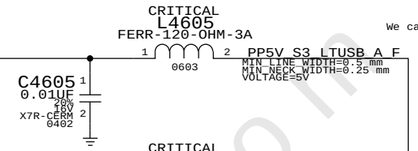
USB Port Power Switch



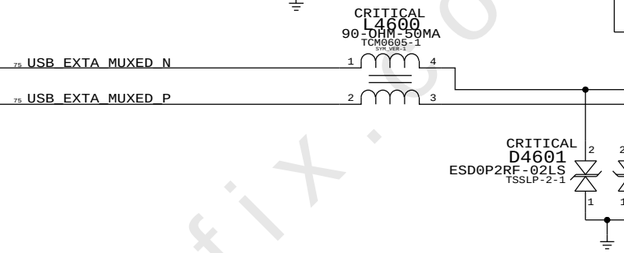
CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

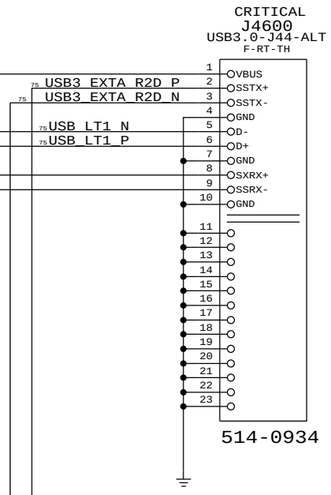
Left USB Port A



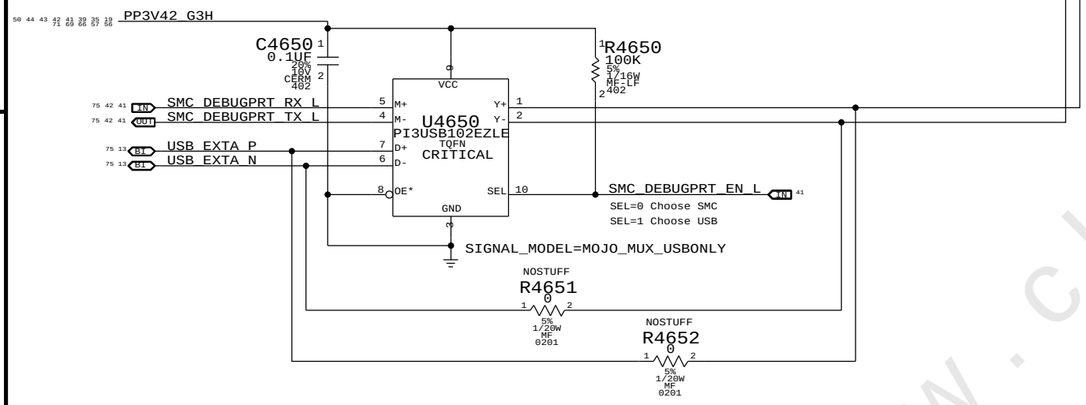
We can add protection to 5V if we want, but leaving NC for now

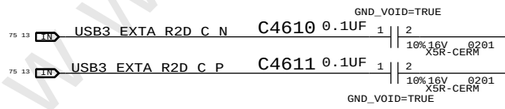
Place L4605 and L4615 at connector pin

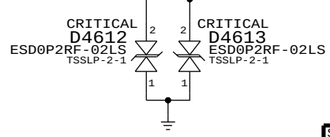




USB/SMC Debug Mux







SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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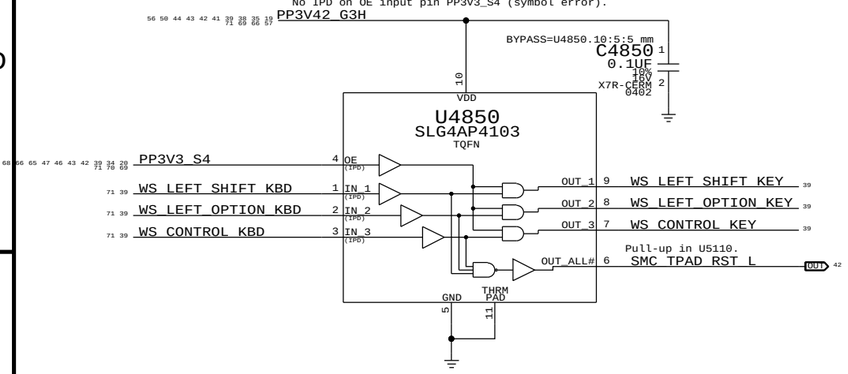
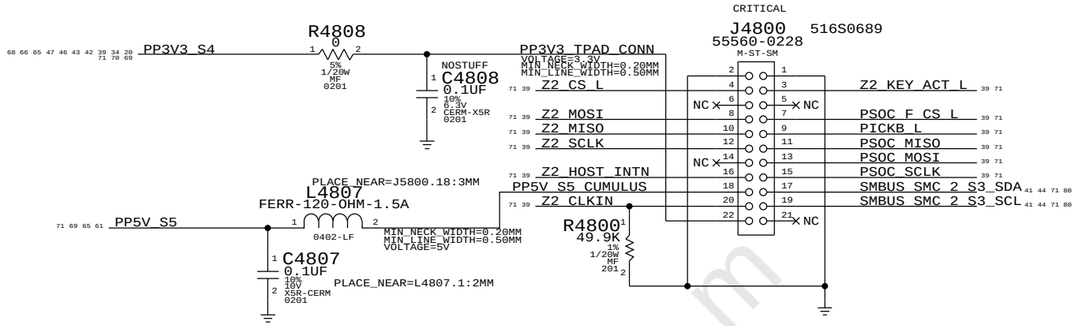
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

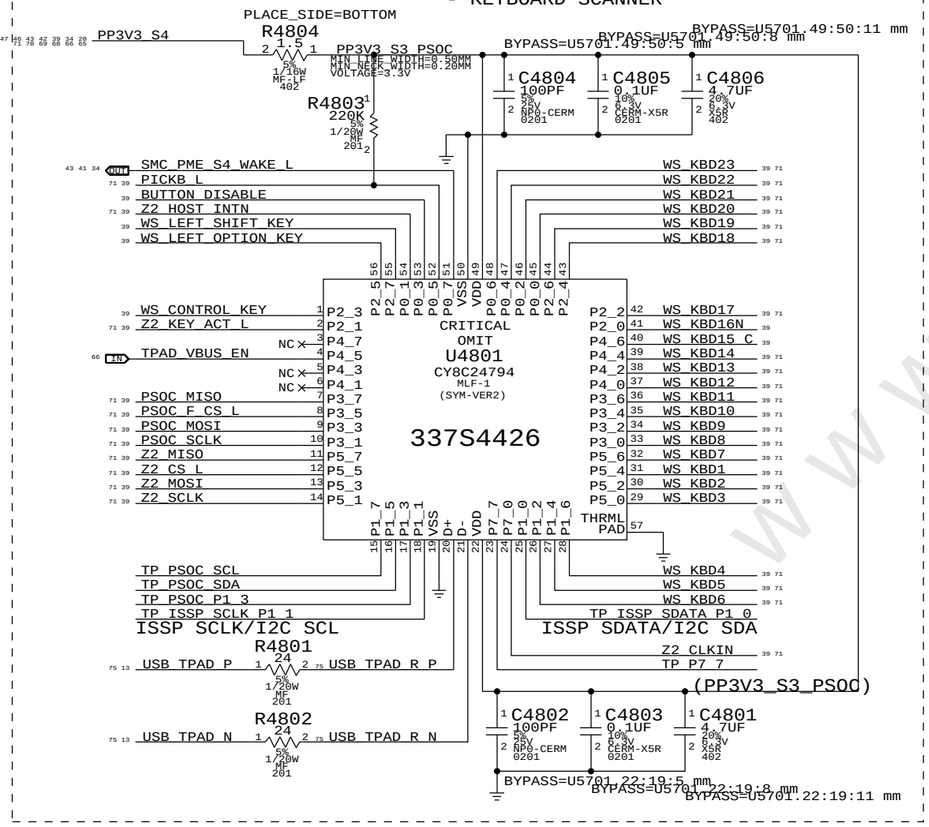


IPD Flex Connector



PSOC USB CONTROLLER

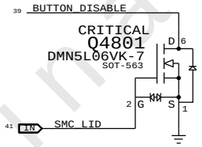
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



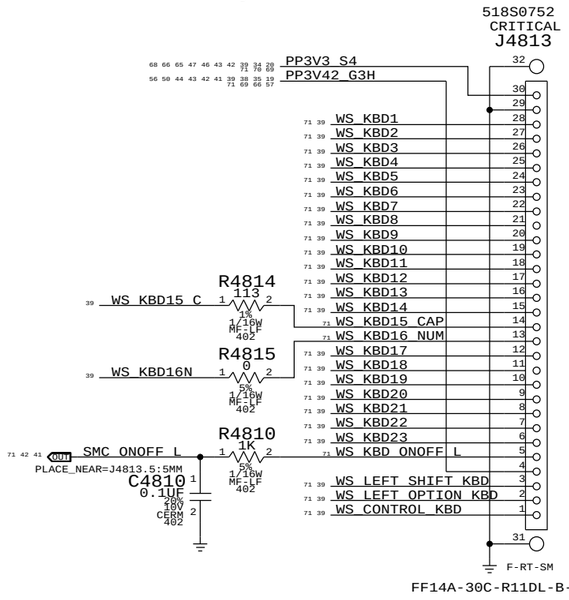
TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V



Keyboard Connector



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

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BRANCH: <BRANCH>
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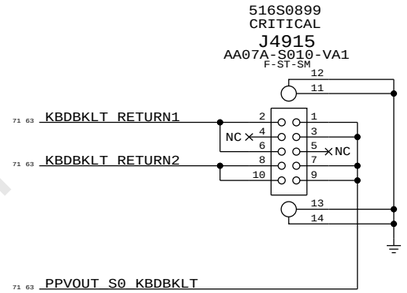
Keyboard Backlight Connector



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PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

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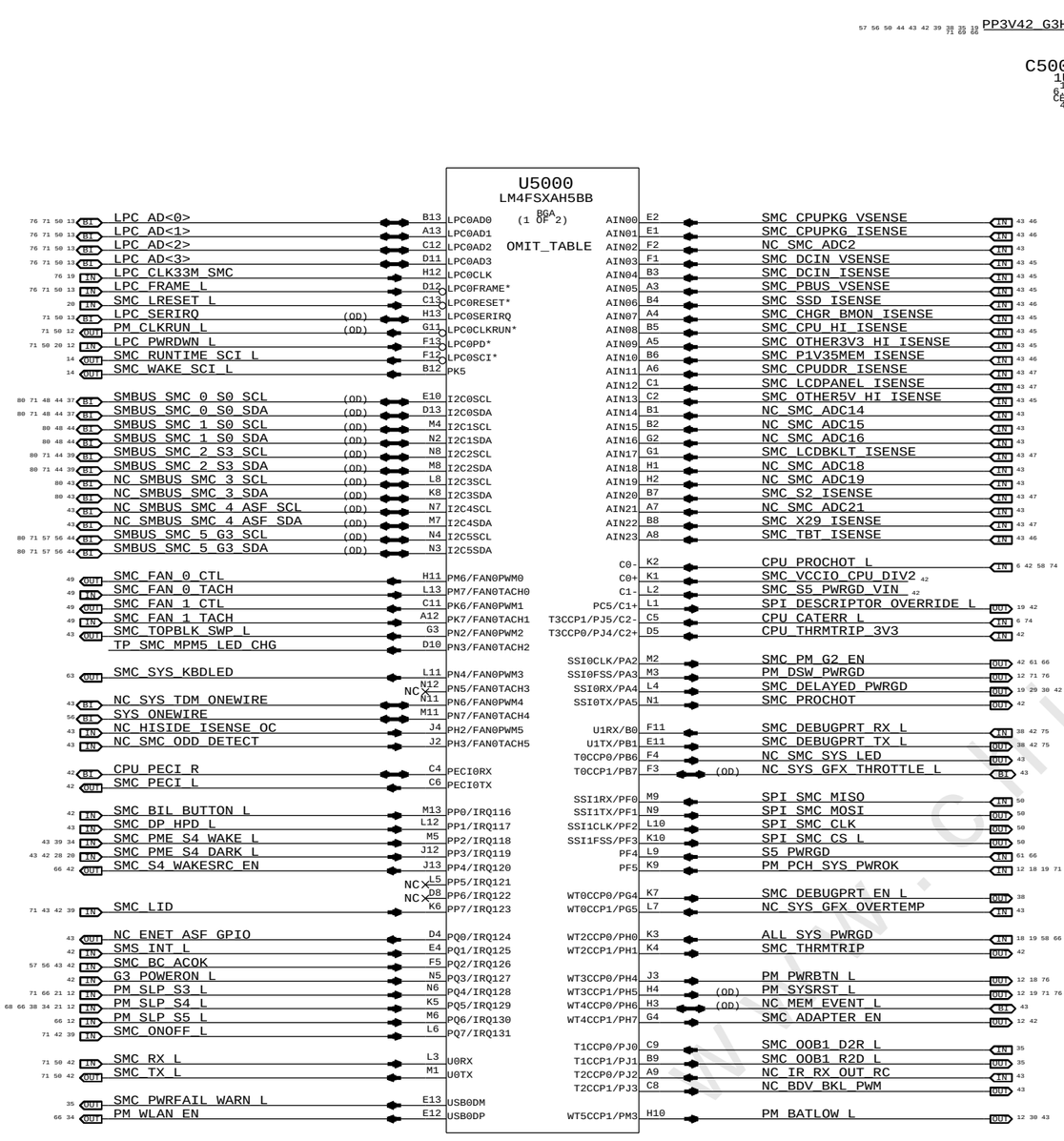
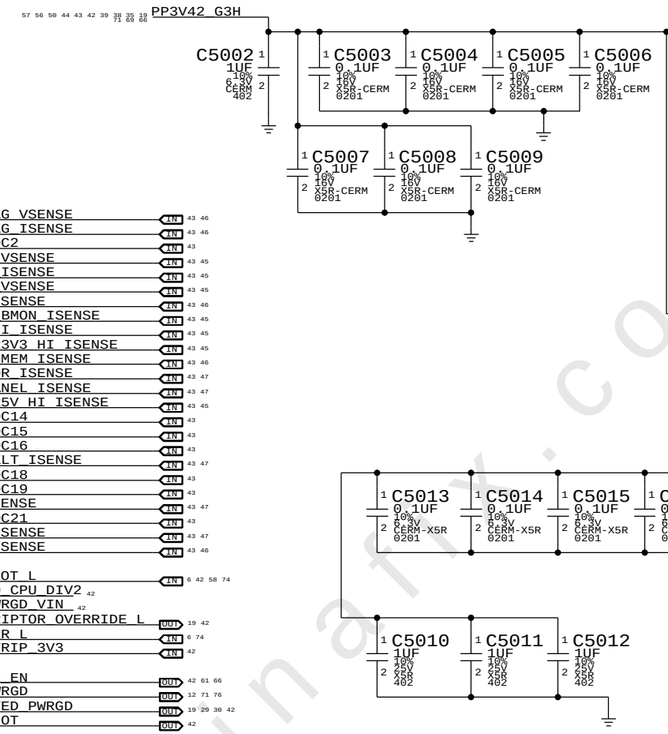
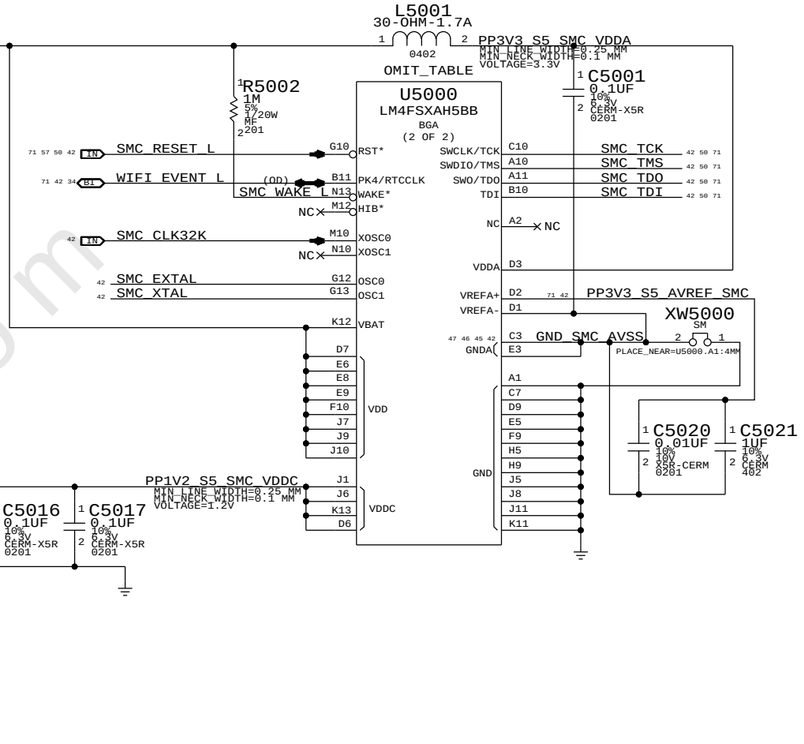
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.







NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: SMC

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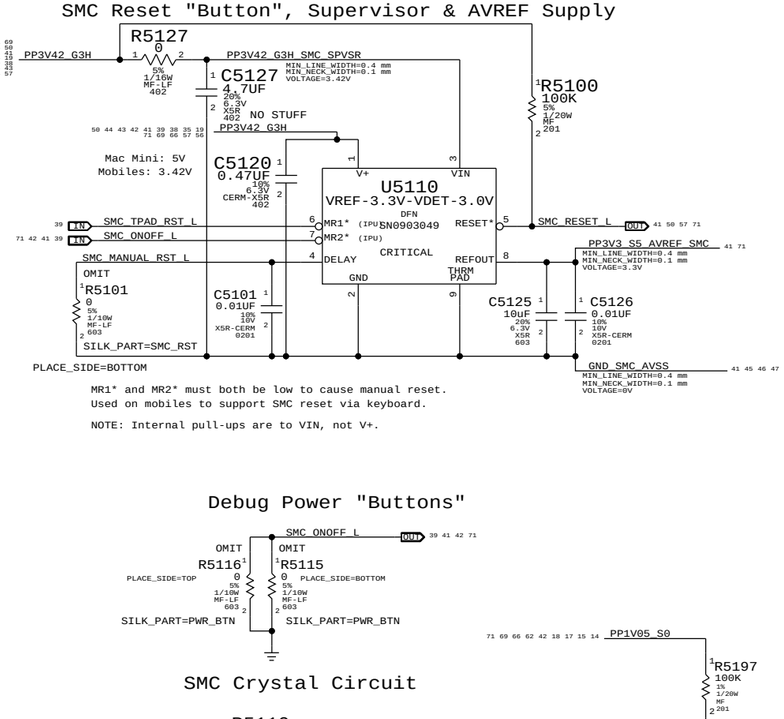
SMC Reset "Button", Supervisor & AVREF Supply

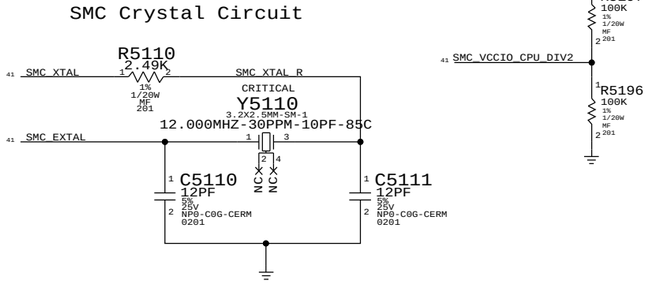


MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

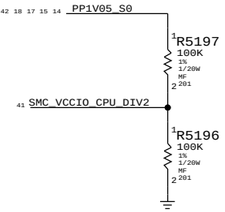
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

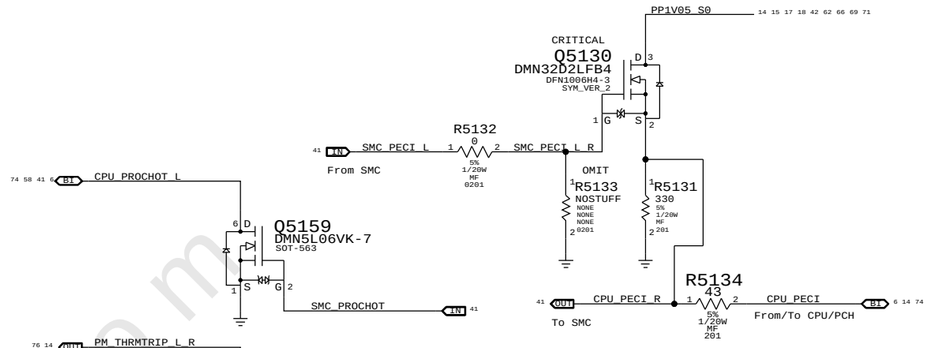
SMC Crystal Circuit

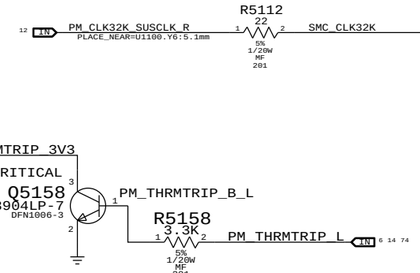


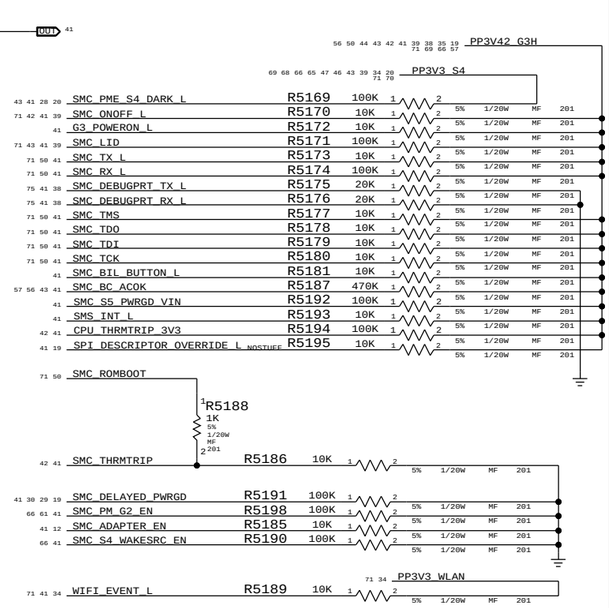
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ



SMC12 PECI SUPPORT







SYNC_MASTER=CHANG_J45 SYNC_DATE=11/12/2012

PAGE TITLE: SMC Shared Support

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SMC_BC_ACOK	SMC_BC_ACOK
NC_HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC
SMC_CPUPKG_VSENSE	SMC_CPUPKG_VSENSE
SMC_CPUPKG_ISENSE	SMC_CPUPKG_ISENSE
NC_SMC_ADC2	NC_SMC_ADC2
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE
SMC_SSD_ISENSE	SMC_SSD_ISENSE
SMC_CHGR_BMON_ISENSE	SMC_CHGR_BMON_ISENSE
SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE
SMC_OTHER3V3_HI_ISENSE	SMC_OTHER3V3_HI_ISENSE
SMC_P1V35MEM_ISENSE	SMC_P1V35MEM_ISENSE
SMC_CPUDDR_ISENSE	SMC_CPUDDR_ISENSE
SMC_LCDPANEL_ISENSE	SMC_LCDPANEL_ISENSE
SMC_OTHER5V_HI_ISENSE	SMC_OTHER5V_HI_ISENSE
NC_SMC_ADC14	NC_SMC_ADC14
NC_SMC_ADC15	NC_SMC_ADC15
NC_SMC_ADC16	NC_SMC_ADC16
SMC_LCDBKLT_ISENSE	SMC_LCDBKLT_ISENSE
NC_SMC_ADC18	NC_SMC_ADC18
NC_SMC_ADC19	NC_SMC_ADC19
SMC_S2_ISENSE	SMC_S2_ISENSE
NC_SMC_ADC21	NC_SMC_ADC21
SMC_X29_ISENSE	SMC_X29_ISENSE
SMC_TBT_ISENSE	SMC_TBT_ISENSE
NC_SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL
NC_SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA
NC_SMBUS_SMC_3_SCL	NC_SMBUS_SMC_3_SCL
NC_SMBUS_SMC_3_SDA	NC_SMBUS_SMC_3_SDA
NC_BDV_BKL_PWM	NC_BDV_BKL_PWM
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L
	SMC_PME_S4_DARK_L

NC_ENET_ASF_GPIO	NC_ENET_ASF_GPIO
NC_SMC_SYS_LED	NC_SMC_SYS_LED
NC_MEM_EVENT_L	NC_MEM_EVENT_L
NC_SMC_ODD_DETECT	NC_SMC_ODD_DETECT
NC_IR_RX_OUT_RC	NC_IR_RX_OUT_RC
NC_SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE
NC_SYS_GFX_THROTTLE_L	NC_SYS_GFX_THROTTLE_L
NC_SYS_GFX_OVERTEMP	NC_SYS_GFX_OVERTEMP

Spare S4 IRQ

PP3V3_S4 → R5259 100K 5% 1/20W MF 201 → SMC_DP_HPD_L (OUT)

Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99
SM

NC, NC, PP3V42_G3H, SMC_LID_R, NC, NC

R5250 0 5% 1/20W MF 0201

SMC_LID

C5250 0.001UF 10% 50V X7R-CERM 0402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

PP3V3_S4 → R5282 100K 5% 1/20W MF 201 → SMC_PME_S4_WAKE_L

SMC_PME_S4_WAKE_L (IN) → SMC_PME_S4_WAKE_L (OUT)

SMC_TOPBLK_SWP_L (IN) → R5283 1K 5% 1/20W MF 201 → PCH_STRP_TOPBLK_SWP_L (OUT)

PM_BATLOW_L (IN) → PM_BATLOW_L (OUT)

PAGE TITLE: SMC Project Support

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PCH SMBus "0" Connections

PP3V3_S0

R5300 1K 5% 1/16W MF-LF 402
R5301 1K 5% 1/16W MF-LF 402

Lynx Point
U1100
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
MAKE_BASE=TRUE

VRef DACs
U2200
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U2201
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J1800 & J1850
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U7100
(WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

PCH "SMLink 0" Connections

PP3V3_S0

R5310 8.2K 5% 1/16W MF-LF 402
R5311 8.2K 5% 1/16W MF-LF 402

Lynx Point
U1100
(MASTER)
- SML_PCH_0_CLK
- SML_PCH_0_DATA
MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF
R5320 8.2K 5% 1/20W MF 201
NO STUFF
R5321 8.2K 5% 1/20W MF 201
R5323 0 5% 1/20W MF 0201
R5322 0 5% 1/20W MF 0201

Lynx Point
U1100
(Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK
- SML_PCH_1_DATA
MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5350 2.0K 5% 1/16W MF-LF 402
R5351 2.0K 5% 1/16W MF-LF 402

SMC
U5000
(MASTER)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

L&R Fin Stack Temp
EMC1412-A: U5860
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

J4002
ALS
(Write: 0x72 Read: 0x73)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5370 1K 5% 1/20W MF 201
R5371 1K 5% 1/20W MF 201

SMC
U5000
(MASTER)
- SMBUS_SMC_2_S3_SCL
- SMBUS_SMC_2_S3_SDA
MAKE_BASE=TRUE

Trackpad
J4801
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_2_S3_SCL
- SMBUS_SMC_2_S3_SDA

SMC "1" SMBUS CONNECTIONS

PP3V3_S0

R5360 1K 5% 1/20W MF 201
R5361 1K 5% 1/20W MF 201

SMC
U5000
(MASTER)
- SMBUS_SMC_1_S0_SCL
- SMBUS_SMC_1_S0_SDA
MAKE_BASE=TRUE

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5870
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_1_S0_SCL
- SMBUS_SMC_1_S0_SDA

X29 TEMP
TMP105: U5823
(WRITE: 0X92 READ: 0X93)
- SMBUS_SMC_1_S0_SCL
- SMBUS_SMC_1_S0_SDA

SMC "5" SMBUS CONNECTIONS

PP3V42_G3H

R5380 2.0K 5% 1/20W MF 201
R5381 2.0K 5% 1/20W MF 201

SMC
U5000
(MASTER)
- SMBUS_SMC_5_G3_SCL
- SMBUS_SMC_5_G3_SDA
MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7100
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_5_G3_SCL
- SMBUS_SMC_5_G3_SDA

Battery
J7050
(Write: 0x16 Read: 0x17)
- SMBUS_SMC_5_G3_SCL
- SMBUS_SMC_5_G3_SDA

SMC "4" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SMC "3" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE: SMBus Connections

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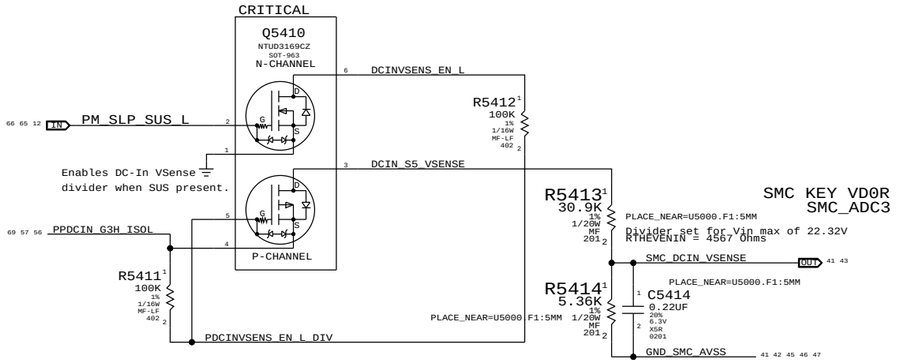
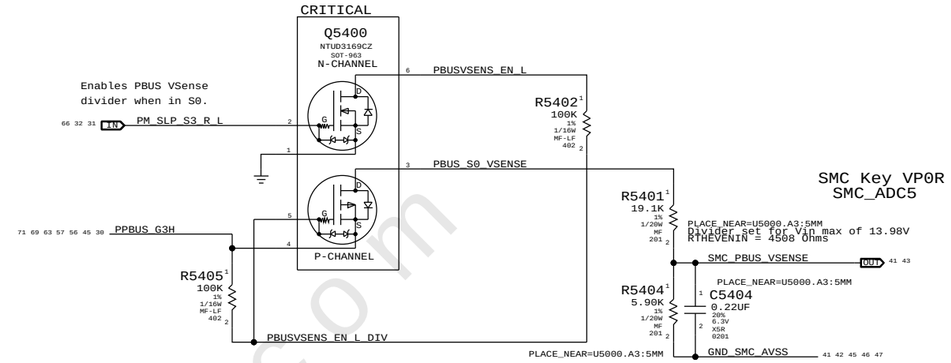
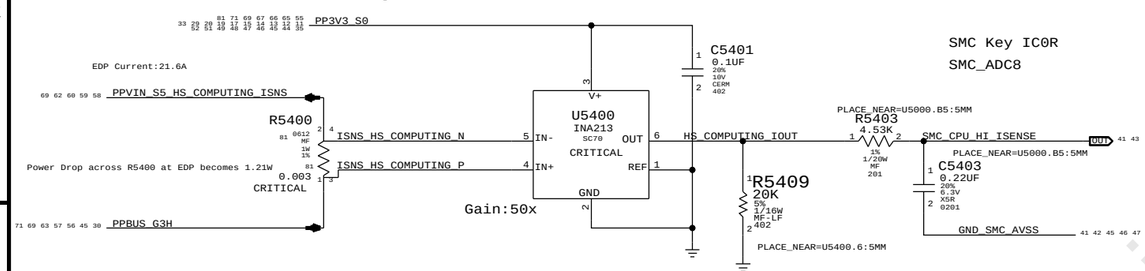
DC-In Voltage Sense Enable & Filter



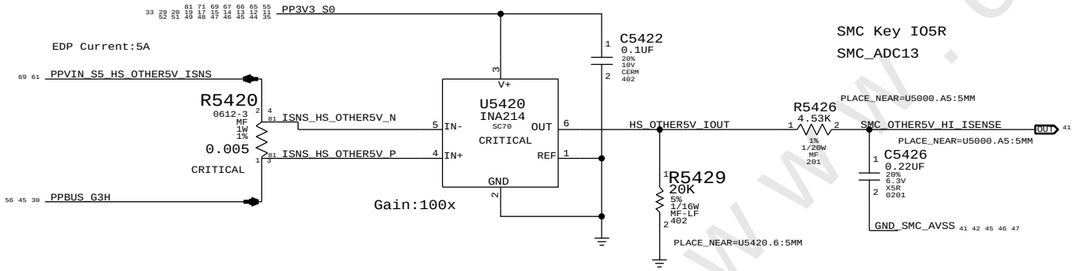
PBUS Voltage Sense Enable & Filter



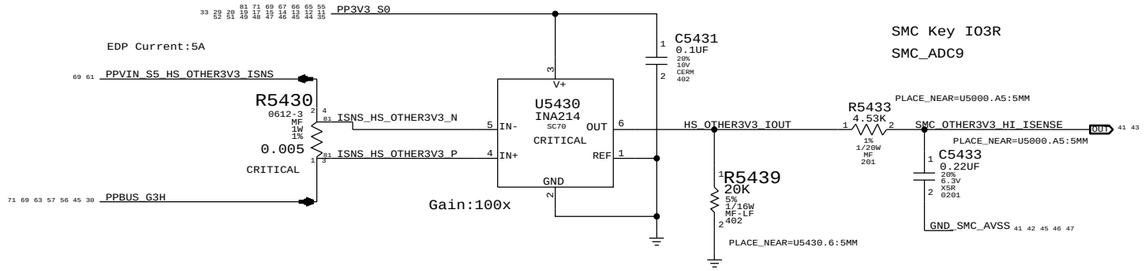
COMPUTING High Side Current Sense / Filter



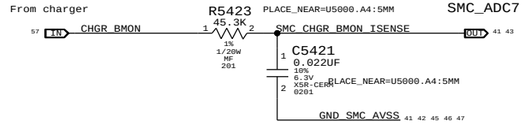
OTHERS (5V) High Side Current Sense / Filter



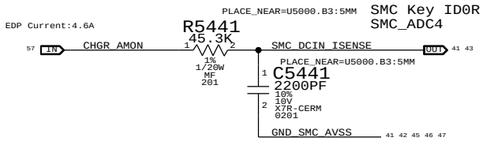
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CHANG_J45 SYNC_DATE=12/21/2012

PAGE TITLE: High Side Voltage and Current Sensing

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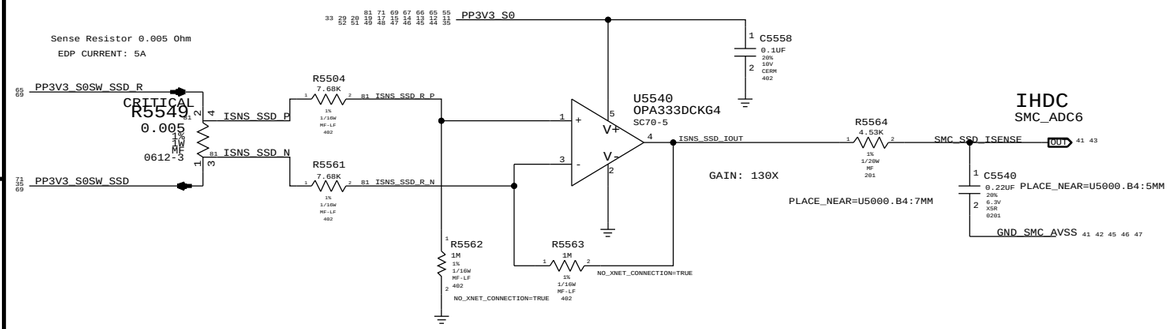
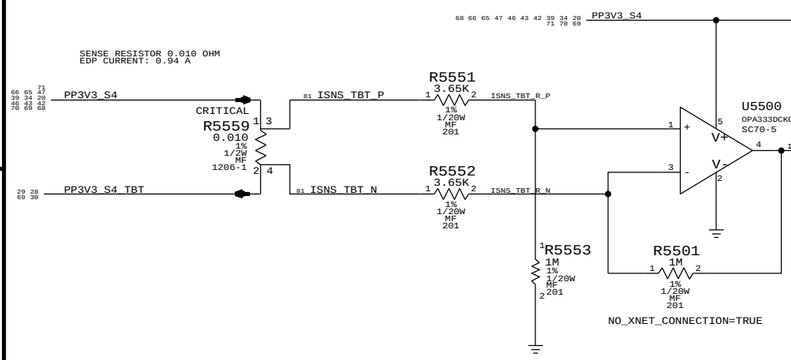
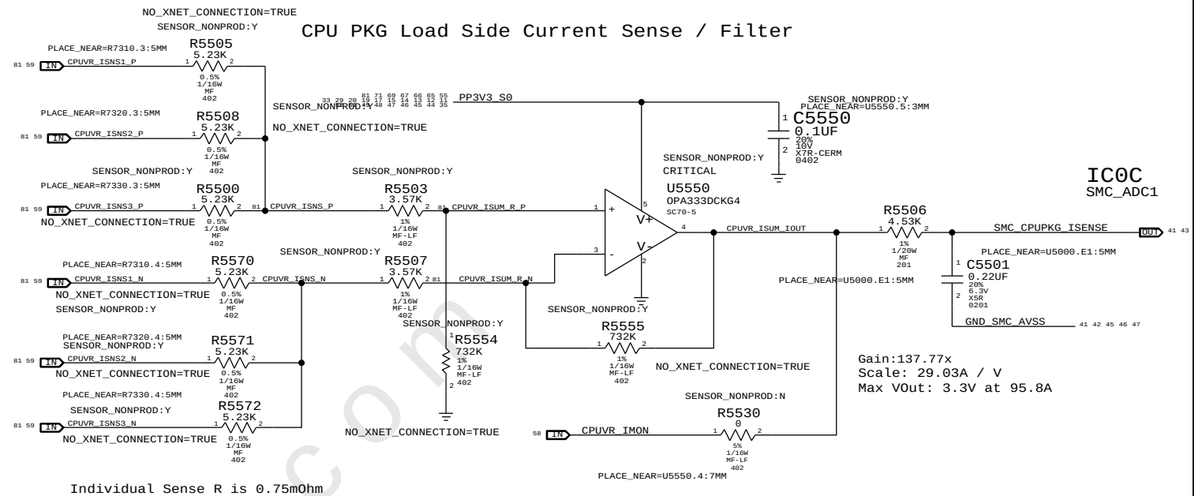
SSD CURRENT SENSE



TBT Router CURRENT SENSE

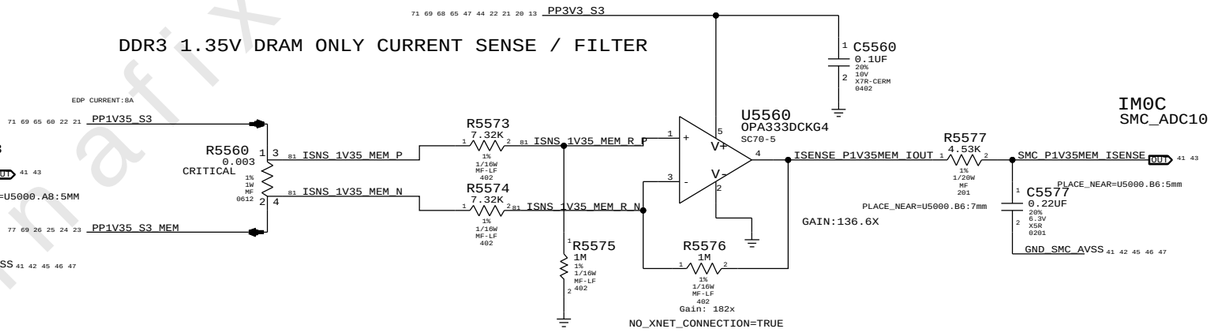


CPU PKG Load Side Current Sense / Filter

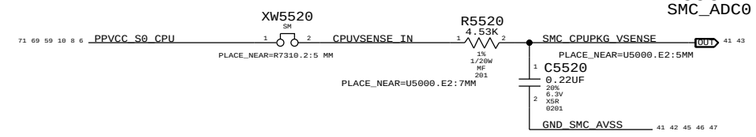


Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER



CPU Vcore Voltage Sense / Filter



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SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: Load Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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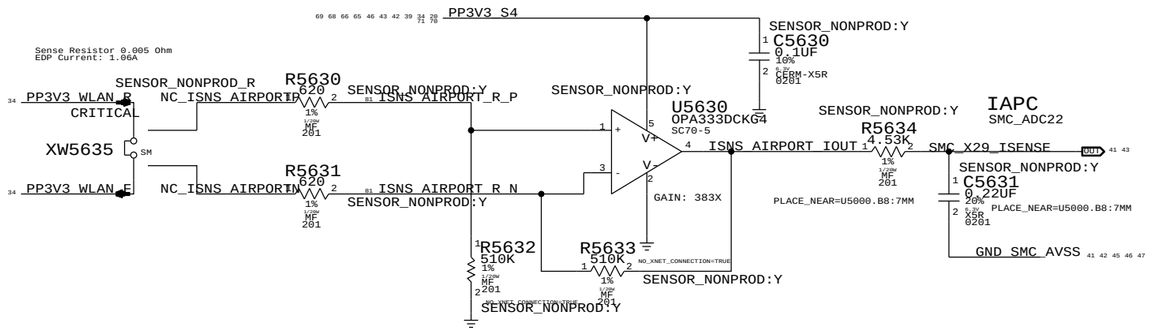
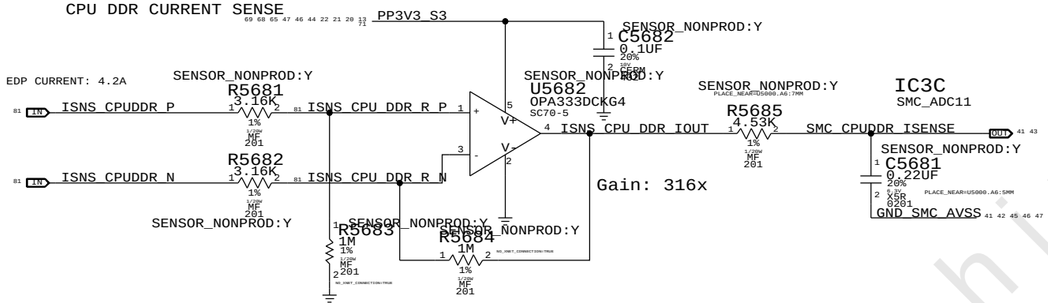
X29 AIRPORT CURRENT SENSE

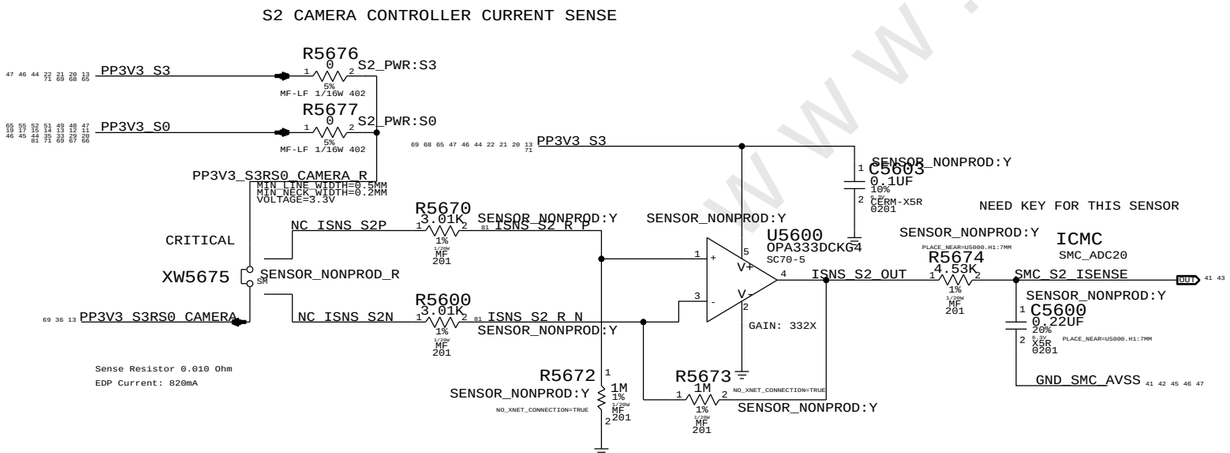


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5600,C5631,C5680,C5681,C5671,C5610		SENSOR_NONPROD:N

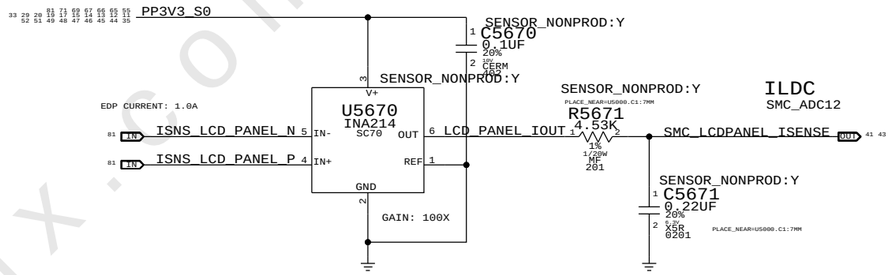
CPU DDR CURRENT SENSE



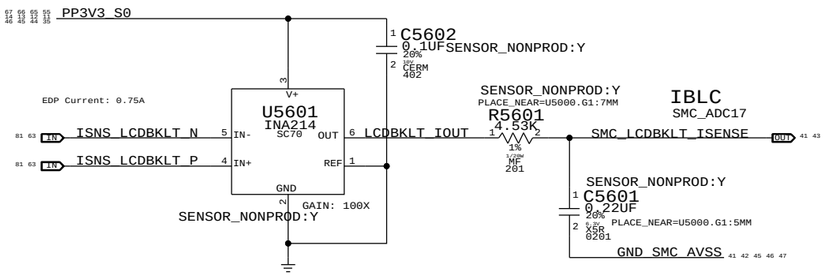
S2 CAMERA CONTROLLER CURRENT SENSE



LCD PANEL CURRENT SENSE



LCD BKLT Current Sense



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SYNC_MASTER=CHANG_J45	SYNC_DATE=12/21/2012
PAGE TITLE	Debug Sensors
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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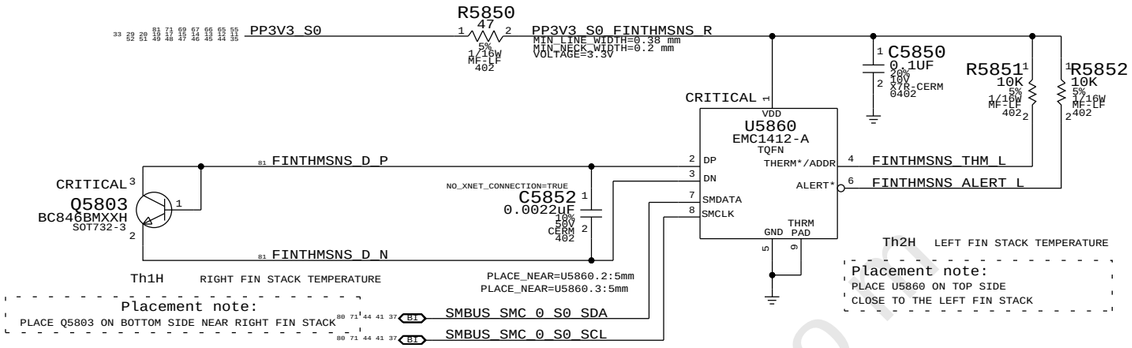
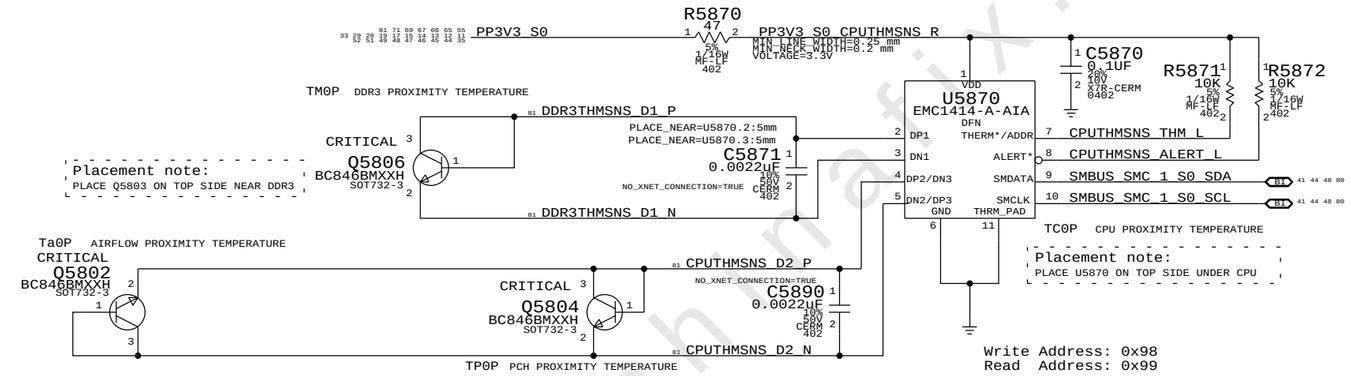
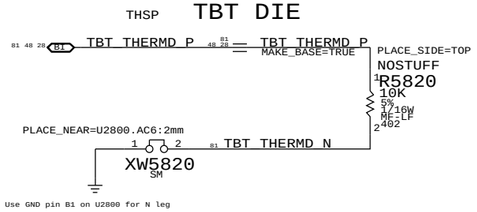
LEFT FIN STACK/RIGHT FIN STACK



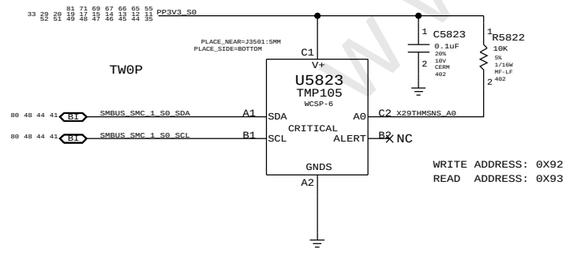
DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



TBT DIE



X29 PROXIMITY



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PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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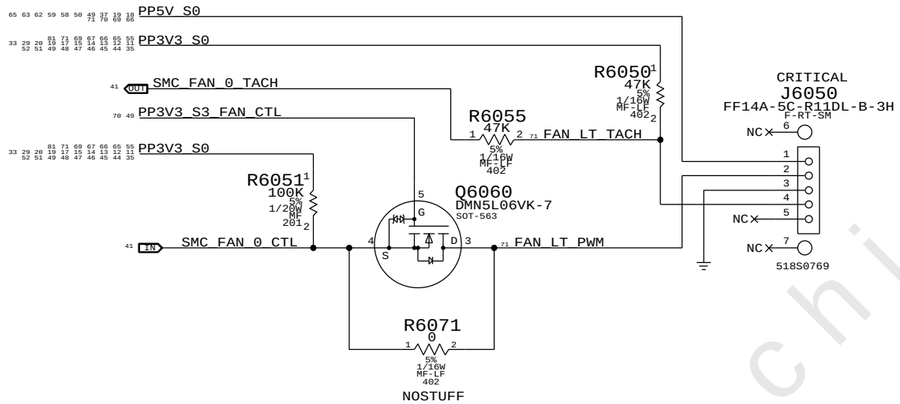
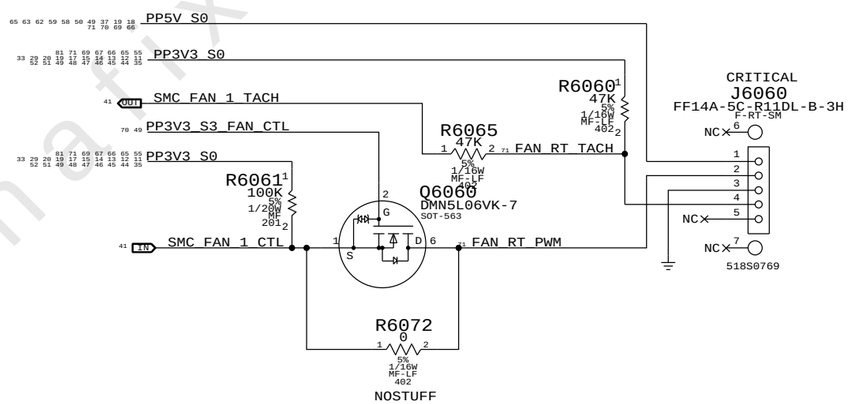
Left Fan



Right Fan



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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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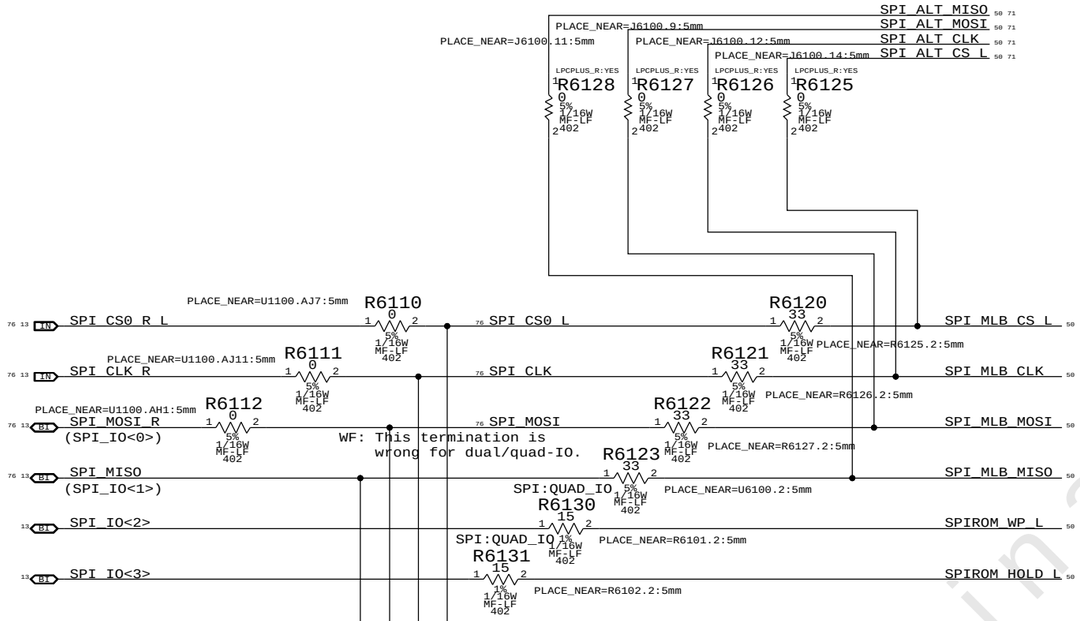
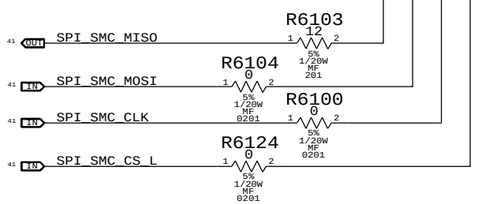
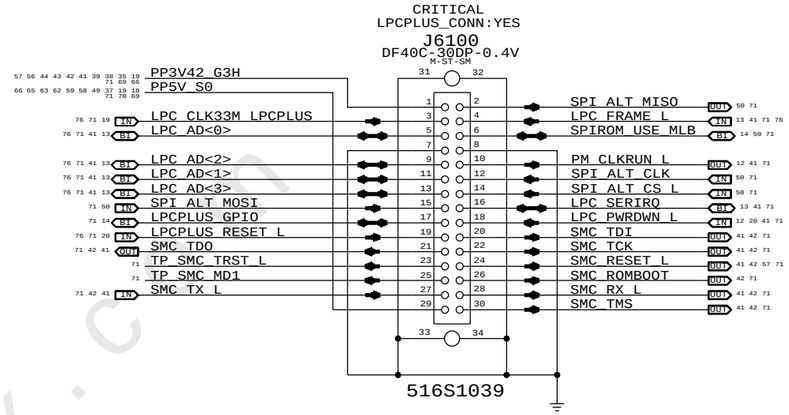
SPI Bus Series Termination



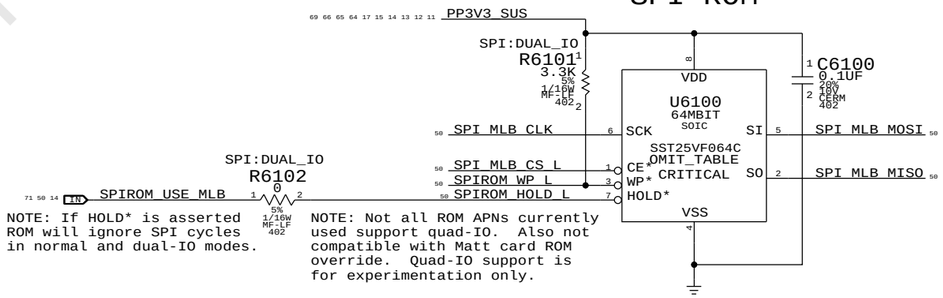
SMC12 SPI SUPPORT



LPC+SPI Connector



SPI ROM



NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and dual-IO modes.

NOTE: Not all ROM APNs currently used support quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: SPI ROM / LPC+SPI Conn.

Apple Inc.

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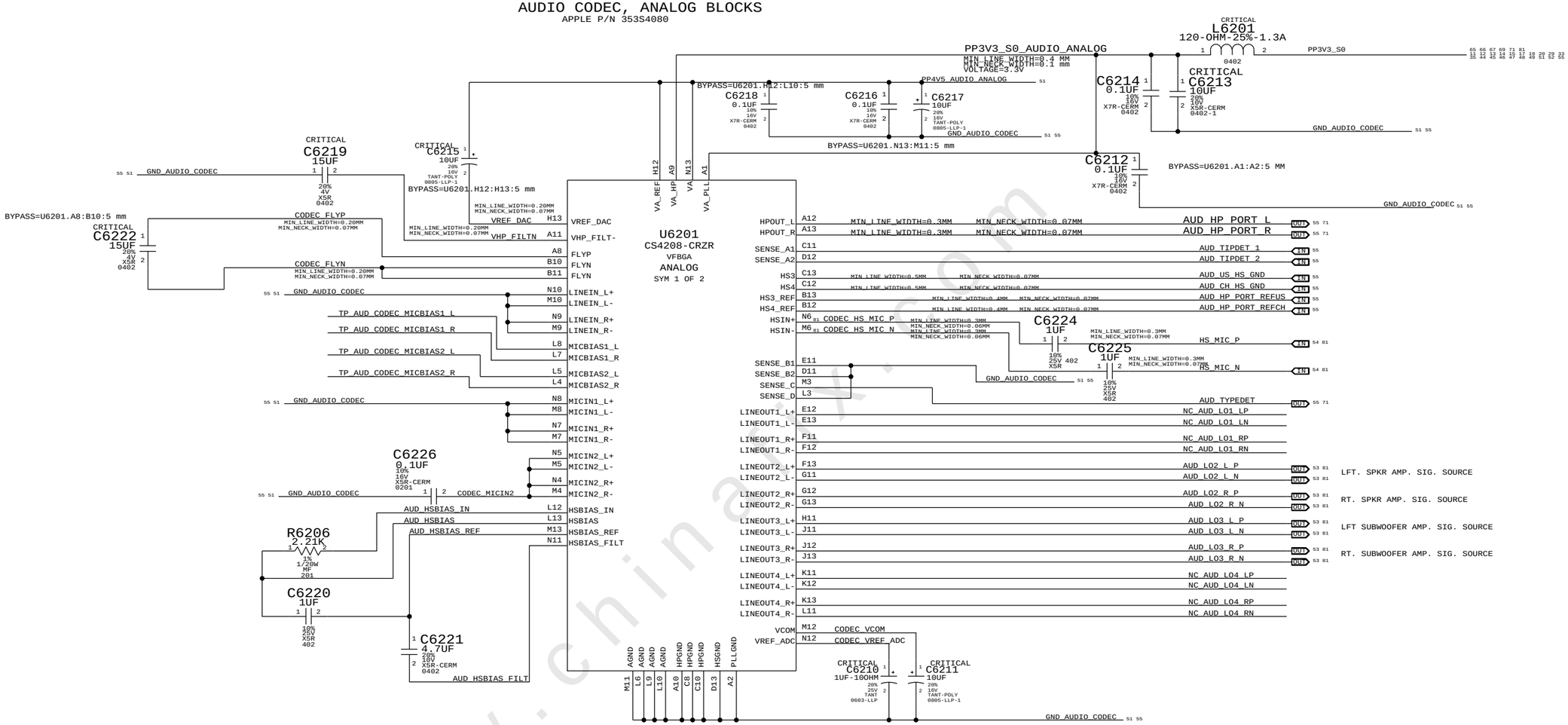
AUDIO CODEC, ANALOG BLOCKS

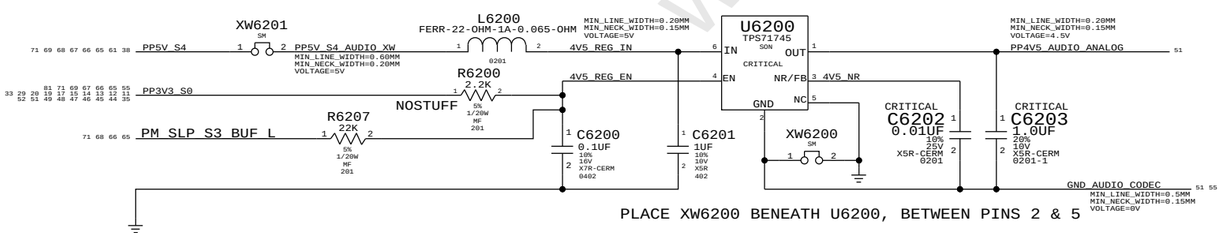
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

SYNC_MASTER=JOE_J45	SYNC_DATE=07/30/2013
PAGE TITLE	AUDIO:CODEC, ANALOG
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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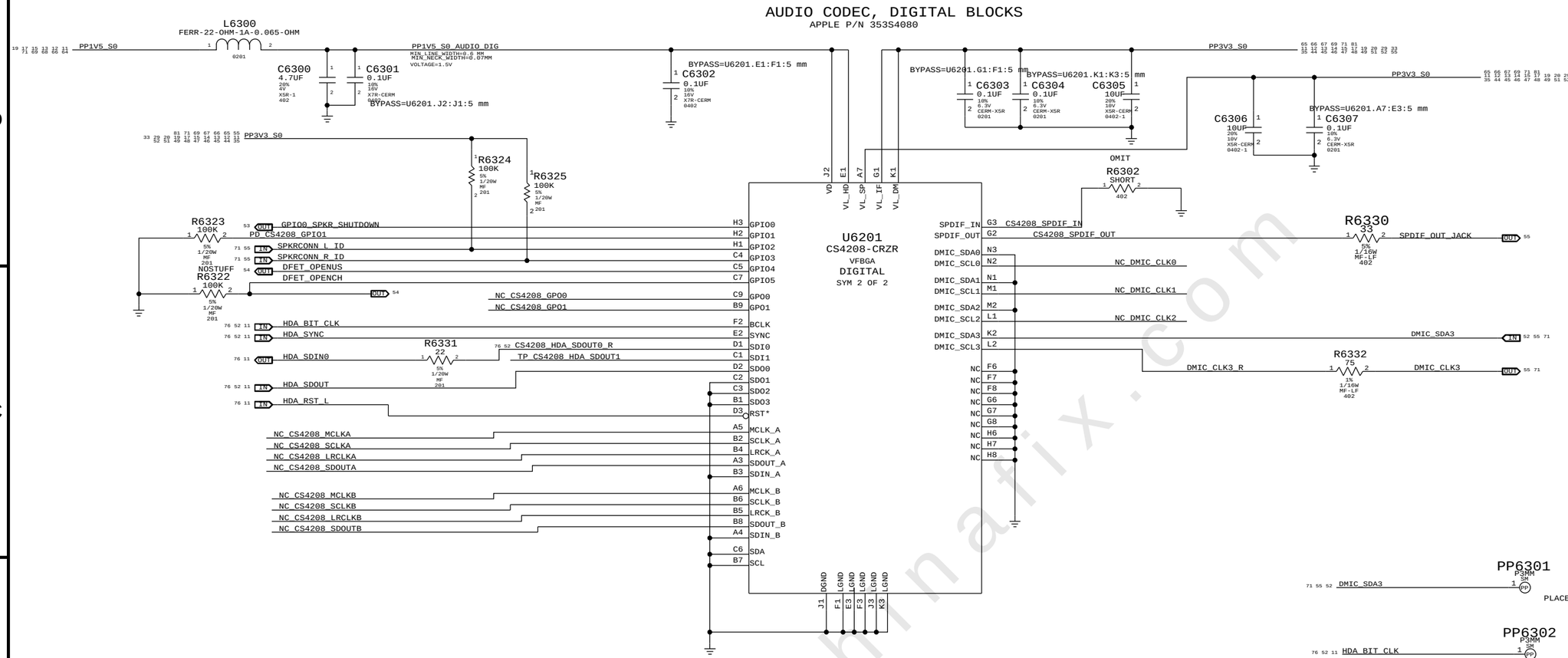
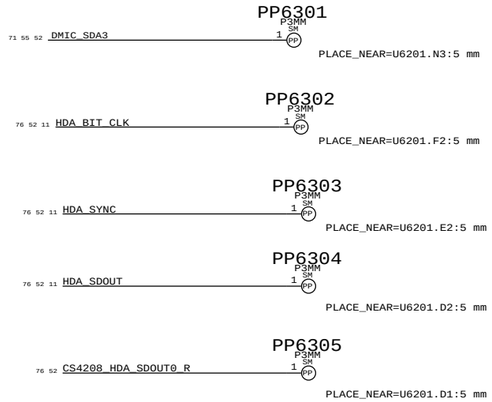
AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080





SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO:CODEC, DIGITAL

Apple Inc.

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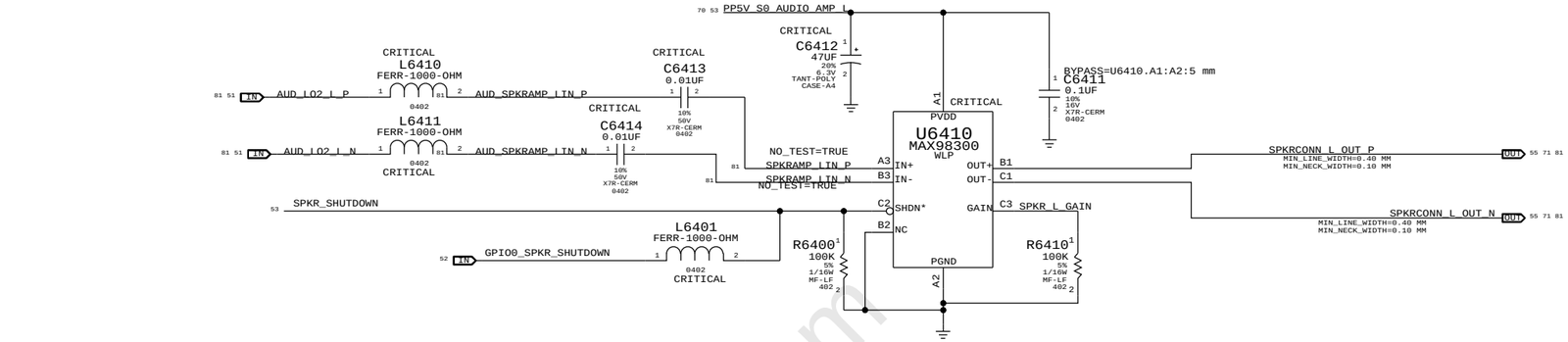
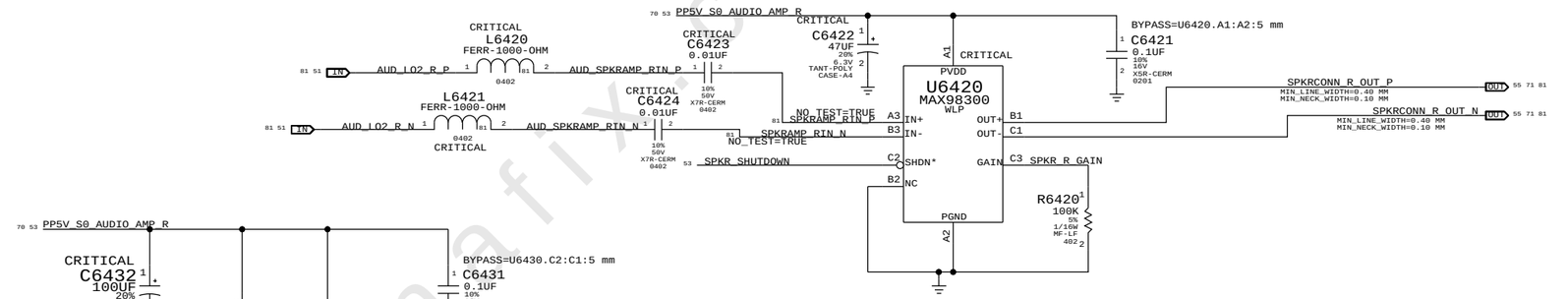
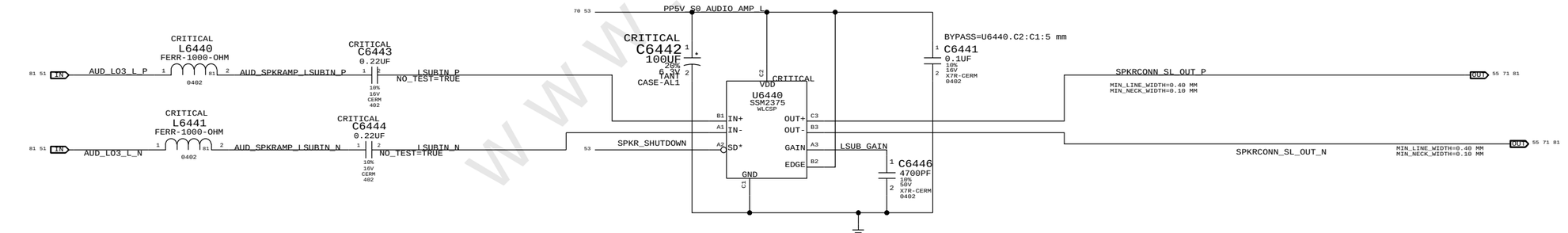
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ







SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

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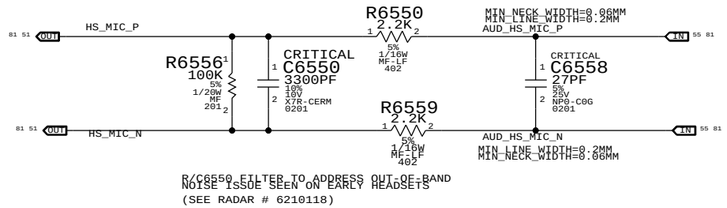

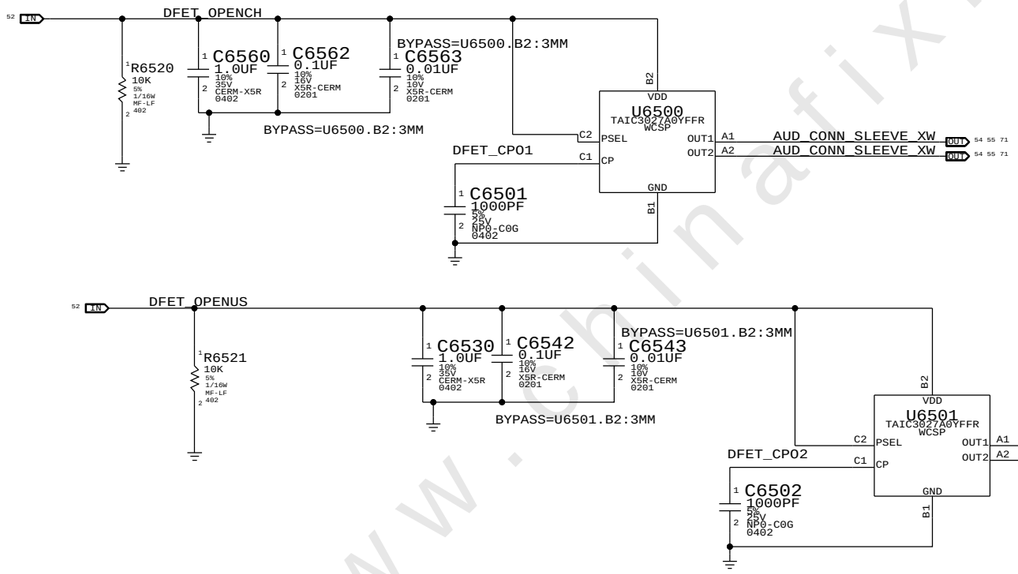

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PAGE TITLE: AUDIO: JACK

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

PP3V3_S0
DMIC_SDA3
DMIC_CLK3
OMIT
R6680
SHORT
DMIC_SDA2

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM
SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603
78171-6006
M-RT-SM
SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N

L6611 120-OHM-25%-1.3A 0402 AUD_HP_PORT_REFCH AUD_CONN_SLEEVE
L6612 120-OHM-25%-1.3A 0402 AUD_CH_HS_GND AUD_CONN_SLEEVE_XW
L6613 120-OHM-25%-1.3A 0402 AUD_HP_PORT_REFUS AUD_CONN_RING2
L6614 120-OHM-25%-1.3A 0402 AUD_US_HS_GND AUD_CONN_RING2_XW
XW6600 SM PLACE_NEAR=J6600.3:2.54mm
XW6601 SM AUD_HS_MIC_P
XW6602 SM PLACE_NEAR=J6600.5:2.54mm
XW6603 SM AUD_HS_MIC_N
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.06MM
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.1MM

L6604 120-OHM-25%-1.3A 0402 AUD_HP_PORT_L AUD_CONN_HP_LEFT
L6605 120-OHM-25%-1.3A 0402 AUD_HP_PORT_R AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.06MM

R6602 2.2K 5% 1/20W MF 201
R6603 2.2K 5% 1/20W MF 201
GND_AUDIO_CODEC

L6608 FERR-470-OHM 0201 AUD_TIPDET_2 AUD_CONN_TIPDET_2
L6607 FERR-470-OHM 0201 AUD_TIPDET_1 AUD_CONN_TIPDET_1
L6606 FERR-470-OHM 0201 AUD_TYPEDET AUD_CONN_TYPEDET

SPDIF_OUT_JACK
PP3V3_S0

R6601 10K 5% 1/16W MF-LF 402

DZ6607 CRITICAL ESDALC5-1BM2 SOD882
DZ6601 CRITICAL ESDALC5-1BM2 SOD882
DZ6602 CRITICAL ESDALC5-1BM2 SOD882
DZ6603 CRITICAL ESDALC5-1BM2 SOD882
DZ6606 CRITICAL ESDALC5-1BM2 SOD882
DZ6605 CRITICAL ESDALC5-1BM2 SOD882
DZ6604 CRITICAL ESDALC5-1BM2 SOD882

C6602 100PF 5% 25V NP0-CERM 0201
C6603 100PF 5% 25V NP0-CERM 0201
C6604 100PF 5% 25V NP0-CERM 0201
C6605 100PF 5% 25V NP0-CERM 0201
C6606 100PF 5% 25V NP0-CERM 0201
C6607 100PF 5% 25V NP0-CERM 0201
C6608 100PF 5% 25V NP0-CERM 0201
C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 6.3V CERM-X5R 0201

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH
MIC
AUDIO GND
2RTN
DET2
DET1
1RTN
R.AUDIO
AUDIO GND
AUDIO
NC
VIN
VDD
GND
OPERATING VOLTAGE 3.3
POF
SHELL PINS

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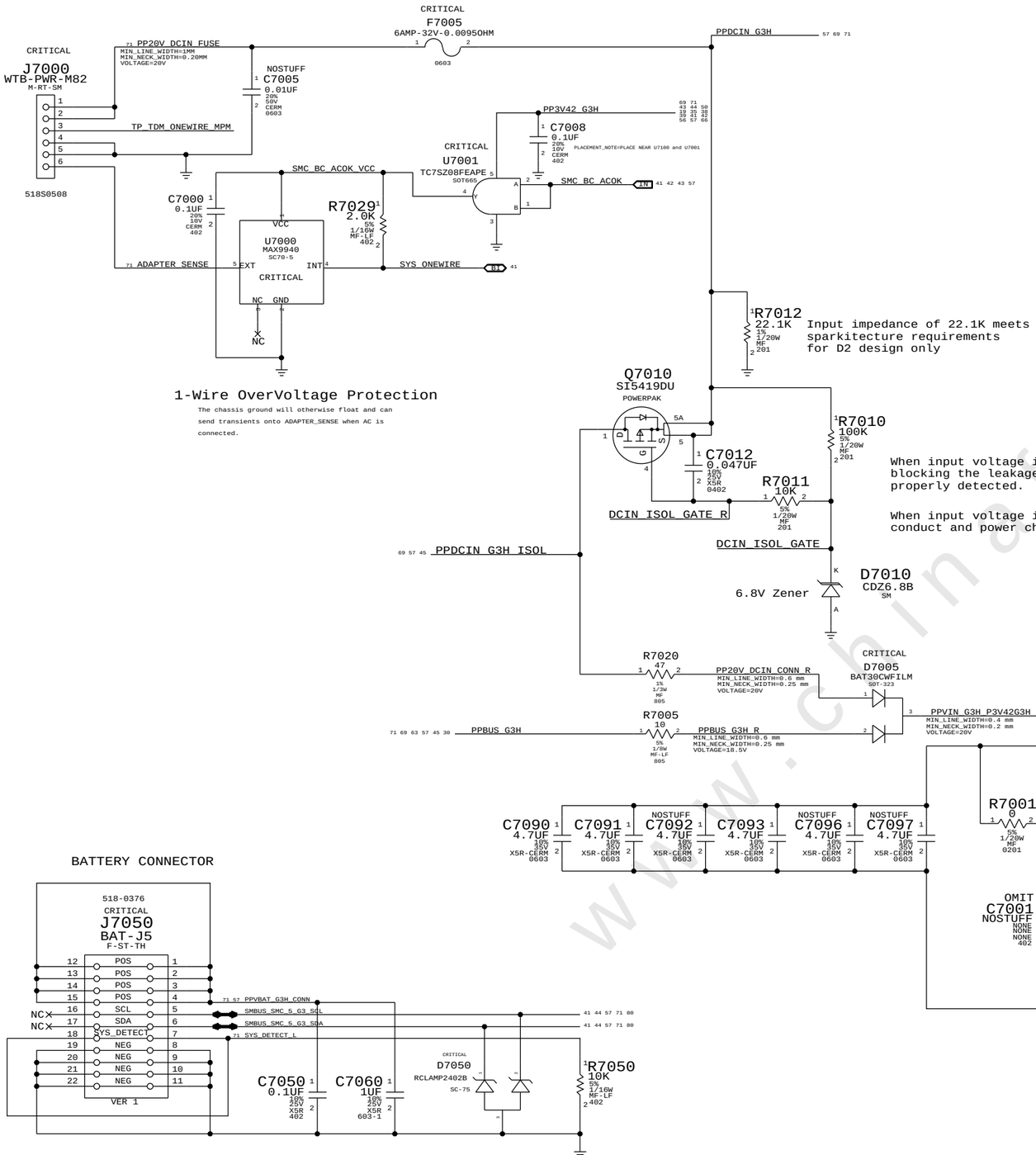
MagSafe DC Power Jack



SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE	DC-In & Battery Connectors
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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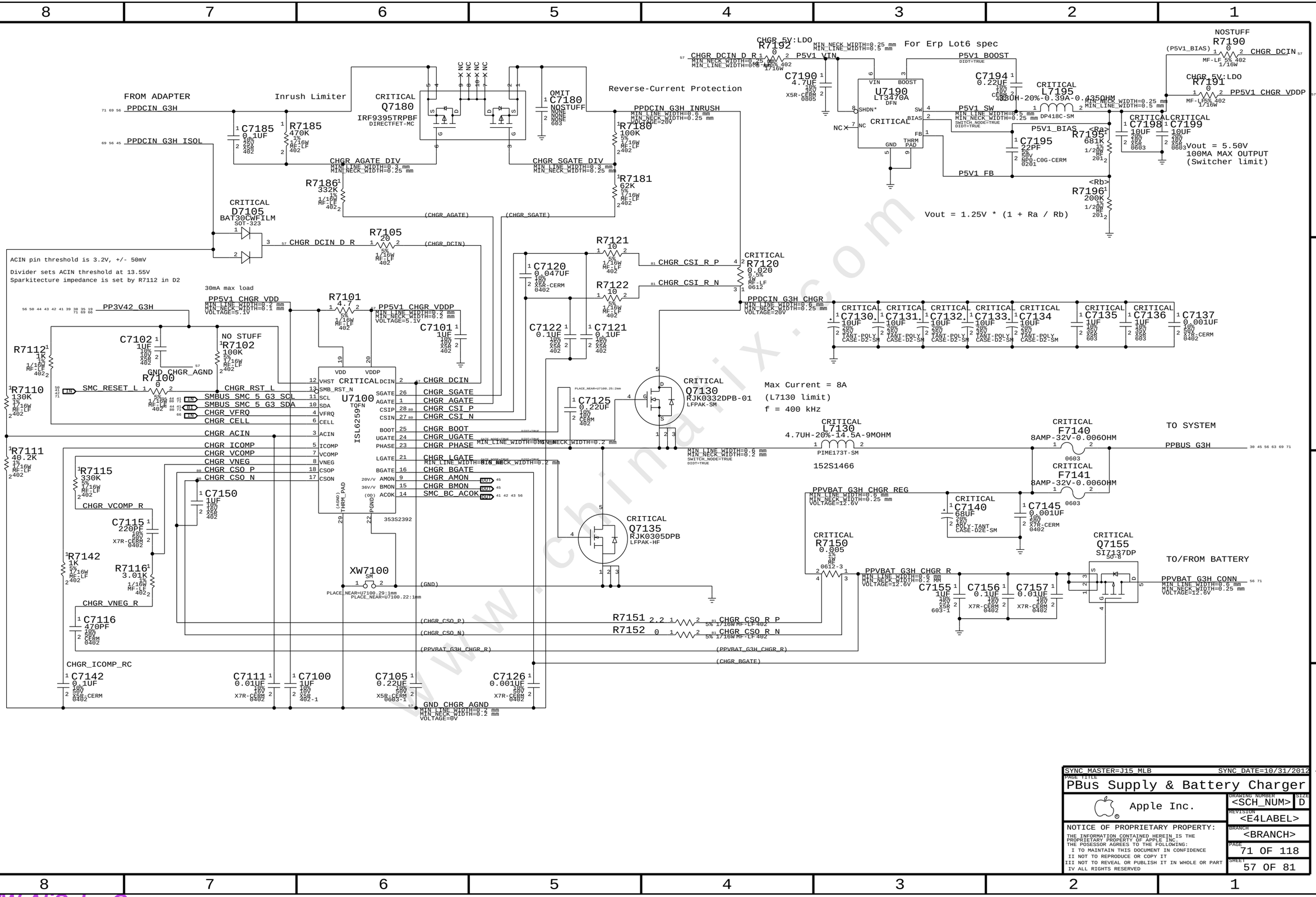

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 71 OF 118
SHEET 57 OF 81

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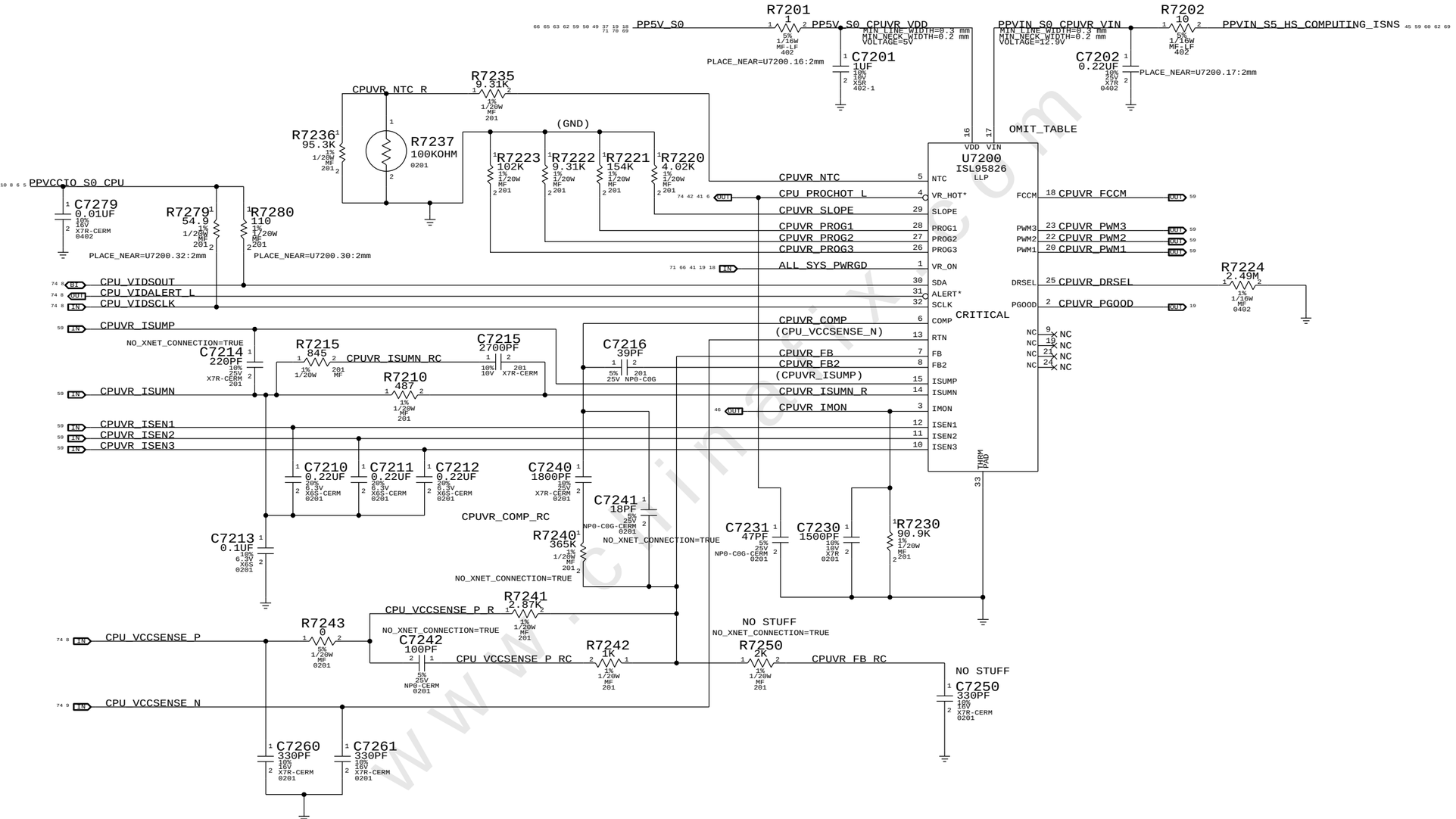
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826R6200,PWM,PGOOD,SCREEN,32P,QFN	U7200	CRITICAL	



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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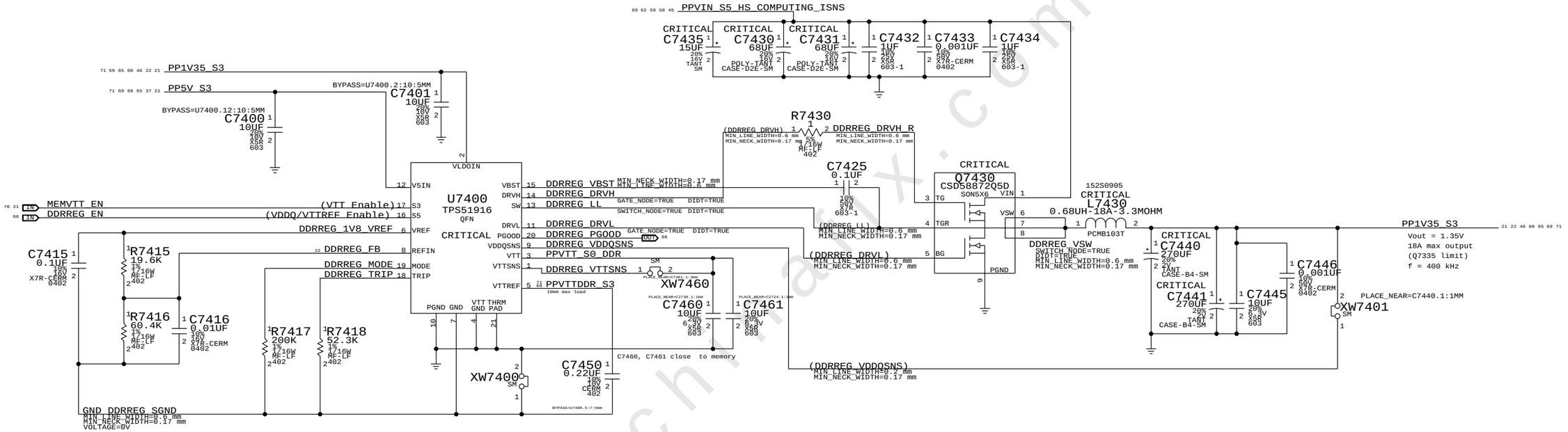
DDR3L (1V35 S3) REGULATOR



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SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE	1.35V DDR3L SUPPLY
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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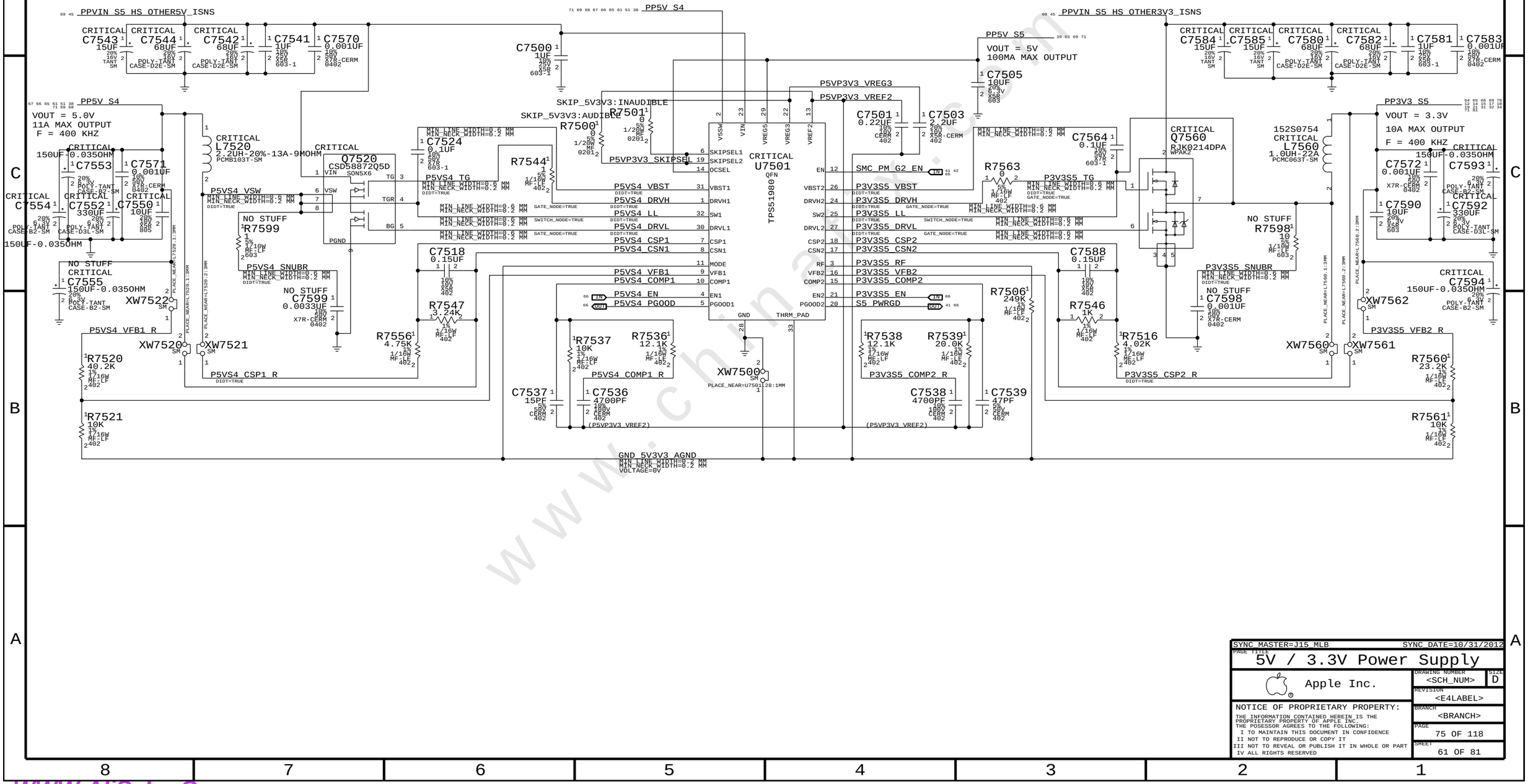

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SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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	BRANCH <BRANCH>
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1V05 S0 REGULATOR

PLACE_NEAR=U1100.AJ12:1MM
XW7601
SM
PP1V05_S0
P1V05S0_SENSE_P
PLACE_NEAR=U1100.AK14:1MM
XW7602
SM
P1V05S0_SENSE_N
Vout = 0.5V * (1 + Ra / Rb)
R7604 3.01K 1% 1/10W MF-LF 402
R7644 3.01K 1% 1/10W MF-LF 402
<Ra>
R7605 2.74K 1% 1/10W MF-LF 402
R7645 2.74K 1% 1/16W MF-LF 402
<Rb>
C7604 10PF 5% 50V C0G-CERM 0402
C7605 10PF 5% 50V C0G-CERM 0402
PPVIN_S5_HS_COMPUTING_ISNS
PP5V_S0
R7601 2.2 5% 1/10W MF-LF 402
C7601 10UF 20% 10V X5R 603
BYPASS=Q9800.14:16:5mm
P1V05S0_BOOT_RC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
DIDT=TRUE
R7630 0 5% 1/10W MF-LF 603
C7630 1UF 10% 10V X5R 402
CRITICAL
C7620 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL
C7621 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7622 1000PF 5% 25V CERM 0402
BYPASS=Q7630.2:5:6mm
PP5V_S0_P1V05S0_VCC
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
U7600
ISL95870
UTQFN
CRITICAL
VCC PVCC
EN FB SREF VO OCSET PGOOD RTN FSEL
BOOT UGATE PHASE LGATE
GND PGND
P1V05S0_EN
P1V05S0_FB
P1V05S0_SREF
P1V05S0_VO
P1V05S0_OCSET
P1V05S0_PGOOD
P1V05S0_RTN
P1V05S0_FSEL
P1V05S0_VBST
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
DIDT=TRUE
P1V05S0_DRVH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
GATE_NODE=TRUE
DIDT=TRUE
P1V05S0_LL
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE
P1V05S0_DRVL
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
GATE_NODE=TRUE
DIDT=TRUE
376S0953
CRITICAL
Q7630
RJK0214DPA
WPAK2
CRITICAL
L7630
0.68UH-25A-5.5MOHM
PCMC063T-SM
152S0955
CRITICAL
R7640 0.001 1% 1W MF-1 0612
PP1V05_S0_REG_R2
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
PP1V05_S0
Vout = 1.05V
12A MAX OUTPUT
f = 300 kHz
C7623 1000PF 5% 25V CERM 0402
PLACE_NEAR=L7630.2:1.5mm
CRITICAL
C7649 270UF 20% 2V TANT CASE-B4-SM
CRITICAL
C7648 270UF 20% 2V TANT CASE-B4-SM
P1V05S0_CS_P
P1V05S0_CS_N
R7641 1.2K 5% 1/16W MF-LF 402
C7640 0.0018UF 10% 50V X7R-CERM 0402
R7642 1.2K 5% 1/16W MF-LF 402
(PCHVCCIOS0_OCSET)
(PCHVCCIOS0_VO)
OCP = R7641 x 8.5uA / R7640
OCP = 14.4A
R7603 0 5% 1/16W MF-LF 402
NO STUFF
C7602 2.2UF 10% 16V X5R 603
BYPASS=Q9800.13:1:5mm
C7603 0.047UF 10% 16V X7R-CERM 0402
P1V05S0_AGND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V
XW7600
SM
PLACE_NEAR=U7600.1:1mm

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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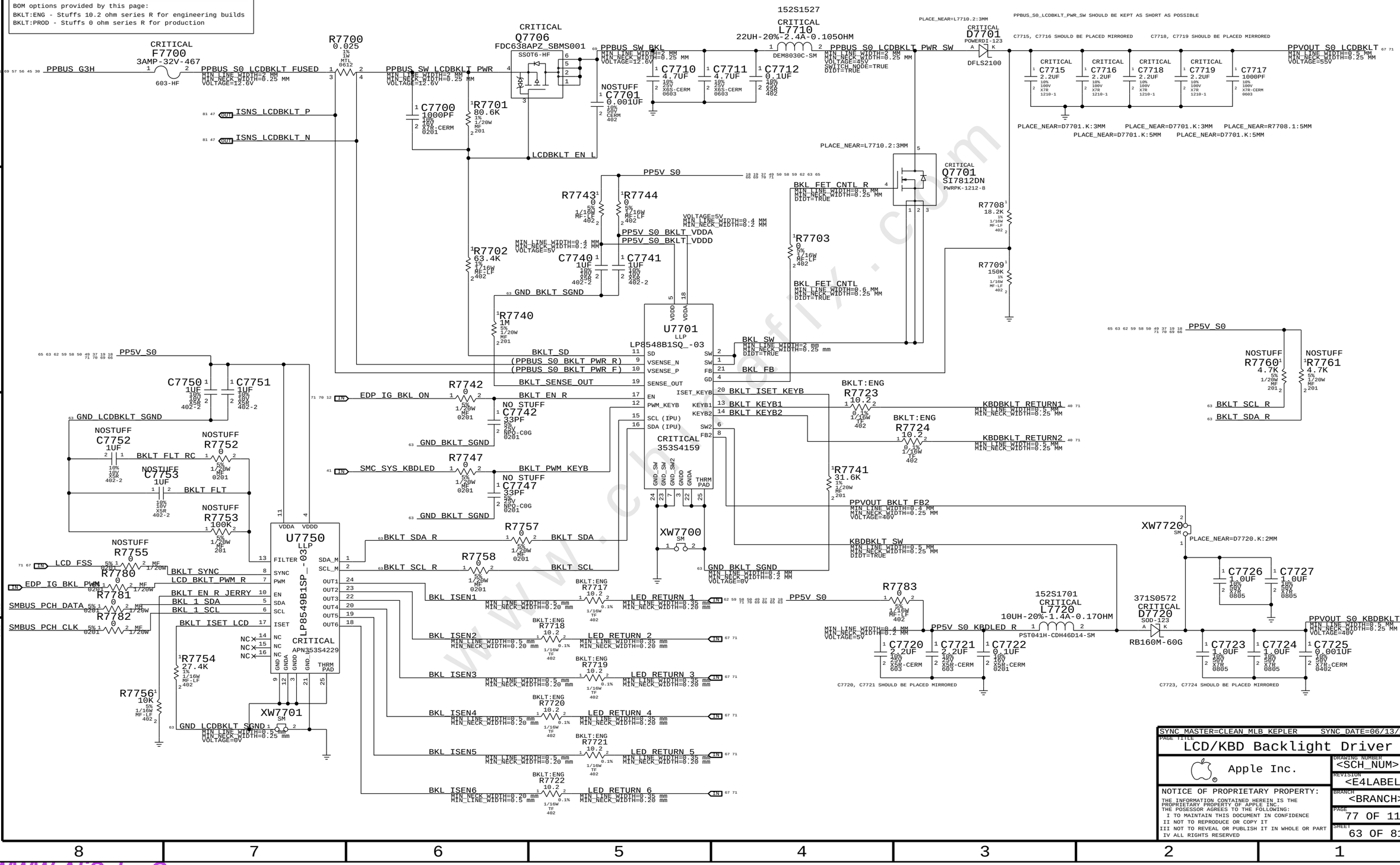
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7717,R7718,R7719,R7720,R7721,R7722,R7723,R7724		BKLT:PROD



SYNC_MASTER=CLEAN_MLB_KEPLER SYNC_DATE=06/13/2013

PAGE TITLE
LCD/KBD Backlight Driver

Apple Inc.

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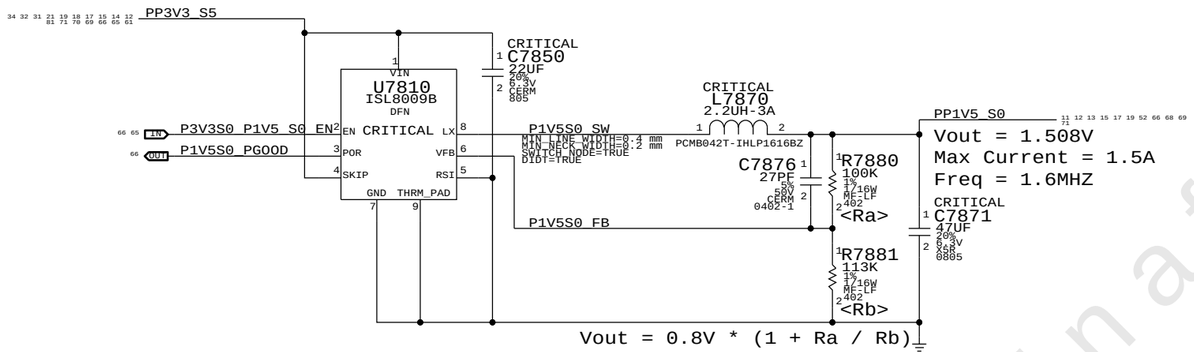
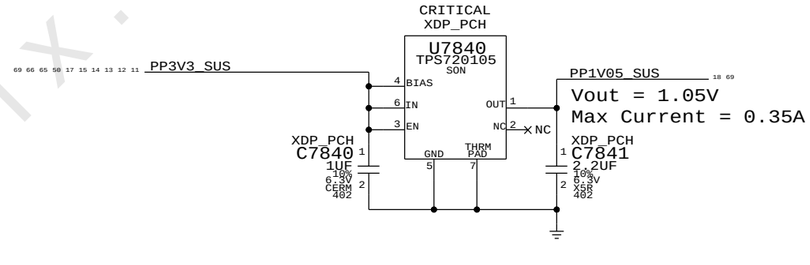
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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3.3V S4 FET

376S0945
CRITICAL
Q8000
SIA413DJ
SC70-6L

EDP is per J45 Power Budget rev5

PP3V3_S5 → R8002 220K → P3V3S4_EN_L → R8000 47K → P3V3S3_S4 → PP3V3_S4
C8009 0.033UF 10% 16V X5R 402
C8000 0.01UF 10% 16V X7R-CERM 0402
Q8002 DMN5L06VK-7 SOT-563
S4_PWR_EN

3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

CRITICAL
Q8010
SIA413DJ
SC70-6L

PP3V3_S5 → R8012 47K → P3V3S3_EN_L → R8010 39K → P3V3S3_SS → PP3V3_S3
C8011 0.033UF 10% 16V X5R 402
C8010 0.01UF 10% 16V X7R-CERM 0402
Q8012 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
P3V3S3_EN

3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

SSD_PWR_EN:GPIO
SSD_PWR_EN → R8073 0 0201 1/20W 5% MF → SSD_PWR_EN_S0 → R8074 0 0201 1/20W 5% MF → PM_SLP_S3_BUF_L
SSD_PWR_FET_EN

5V S3 FET

CRITICAL
Q8050
SIA427DJ
SC70-6L

PP5V_S4 → R8052 200K → P5V3S_EN_L → R8050 5.1K → P5V3S_SS → PP5V_S3
C8051 0.033UF 10% 16V X5R 402
C8050 0.01UF 10% 16V X7R-CERM 0402
Q8052 DMN5L06VK-7 SOT-563
P5V3S_EN

5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

PP5V_S5 → C8001 0.1UF 20% 10V CERM 402
U8001 SLG5AP1438V TDFN CRITICAL
P1V35CPU_SLEW_CTL
CPUVDDQ_EN
C8002 0.018UF 10% 16V X7R 402
Slew rate : 0.8V/ms = 19.75nF
PP1V35_S3

1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SENSOR_NONPROD_R
XW8005 SM
PP1V35_S3RS0_FET → PP1V35_S3RS0_CPUDDR
NC_ISNS_CPUDDRN
NC_ISNS_CPUDDRP

3.3V SUS FET

CRITICAL
Q8020
SIA413DJ
SC70-6L

PP3V3_S5 → R8022 100K → P3V3SUS_EN → R8020 12K → P3V3SUS_SS → PP3V3_SUS
C8021 0.033UF 10% 16V X5R 402
C8020 0.01UF 10% 16V X7R-CERM 0402
Q8002 DMN5L06VK-7 SOT-563
PM_SLP_SUS

3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

PLACE_NEAR=R5549.2:6mm
CRITICAL
Q8070
SI7615DN
PWRPK-1212-8

PP3V3_S5 → R8072 47K → P3V3_SSD_EN_L → R8070 33K → P3V3_SSD_SS → PP3V3_S0SW_SSD_R
C8071 0.033UF 10% 16V X5R 402
C8070 0.01UF 10% 16V X7R-CERM 0402
Q8072 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

CRITICAL
Q8060
SI7615DN
PWRPK-1212-8

PP5V_S4 → R8062 270K → P5V0S0_EN_L → R8060 6.2K → P5V0S0_SS → PP5V_S0
C8061 0.12UF 10% 10.0V X5R 402
C8060 0.47UF 10% 10V X5R 0402
Q8052 DMN5L06VK-7 SOT-563
P5VS0_EN

5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 Switch

U8030
APN 353S2741
PP3V3_S5 → U8030 TPS22924 CSP → PP3V3_S0
P3V3S0_P1V5_S0_EN
C8030 1UF 10% 6.3V X5R 402
Max Current = 2A

U8030	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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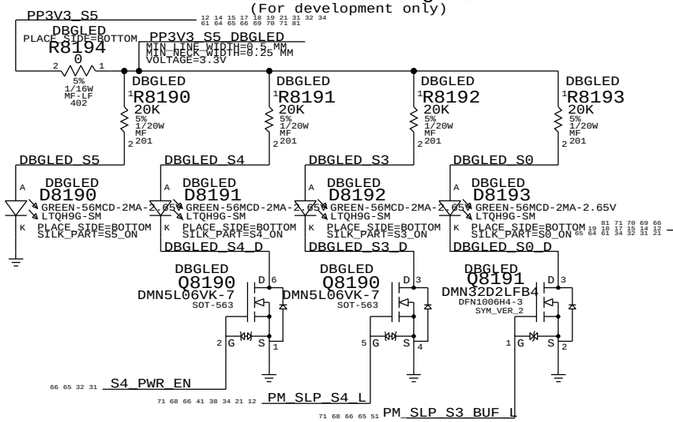
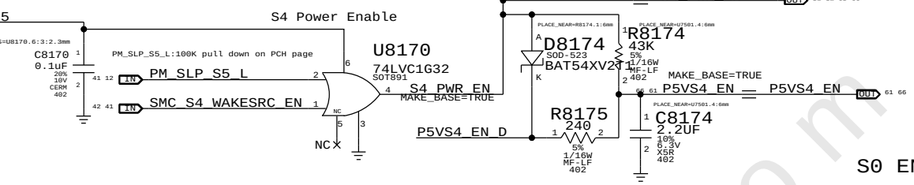
Power State Debug LEDs
(For development only)



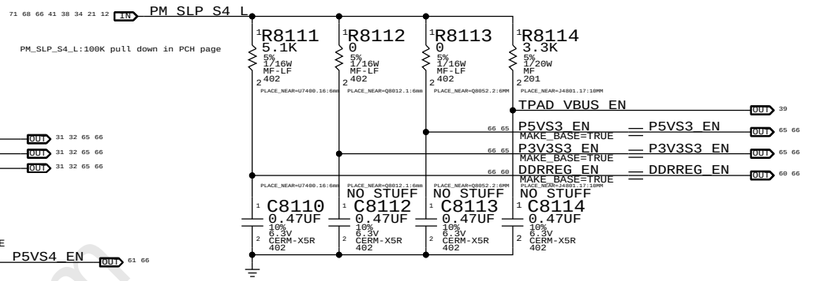
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

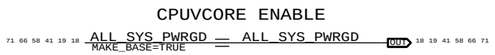
S4 Power Enable



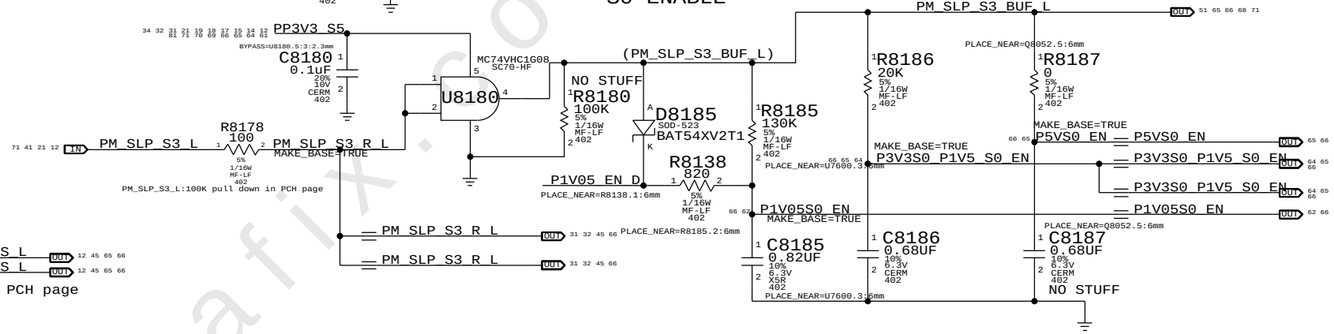
S3 ENABLE



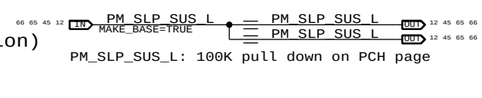
CPUVCORE ENABLE



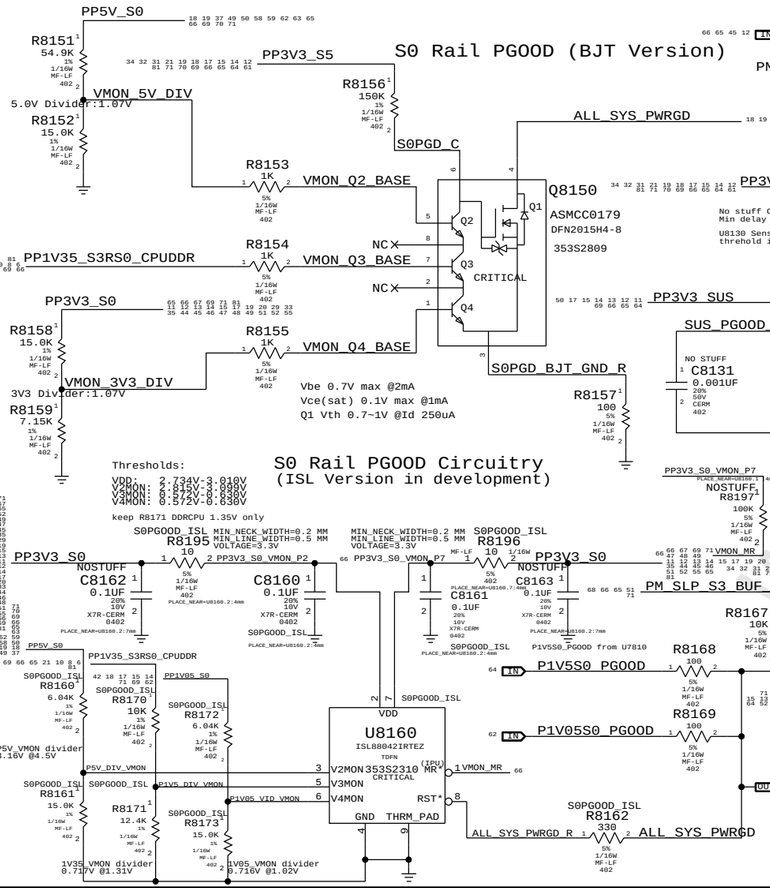
S0 ENABLE



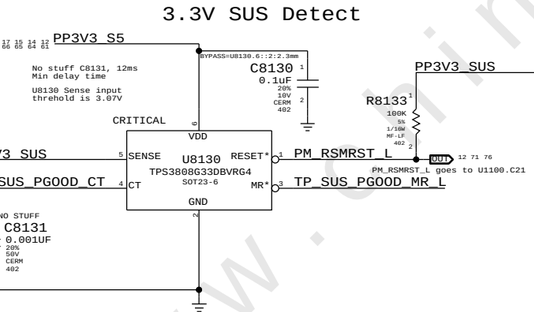
3.3V SUS Enable



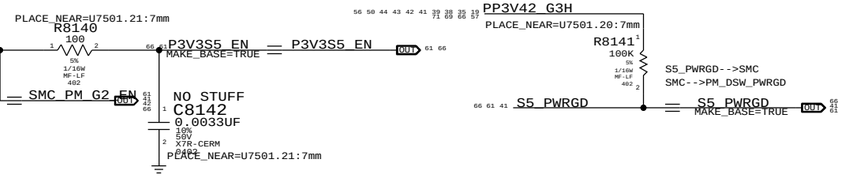
S0 Rail PGOOD (BJT Version)



3.3V SUS Detect

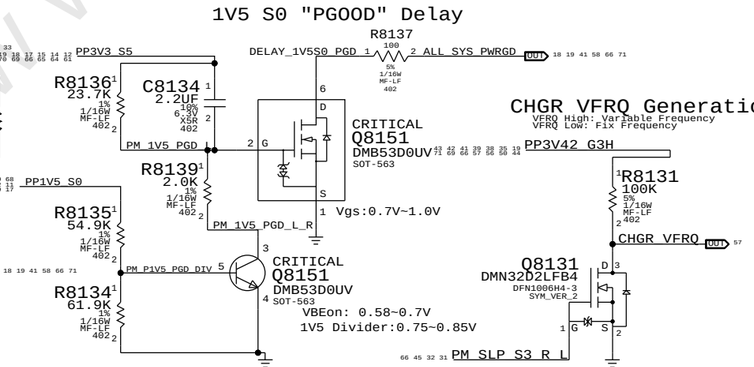


S5 Rail Enables & PGOOD



S0 Rail PGOOD Circuitry
(ISL Version in development)

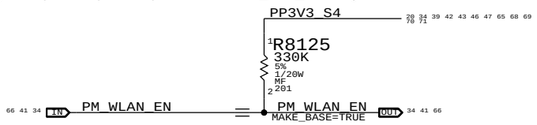
1V5 S0 "PGOOD" Delay



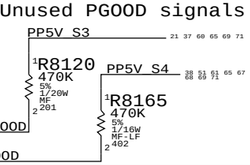
CHGR VFRQ Generation

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.



Unused PGOOD signals



SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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LCD PANEL INTERFACE (eDP)

LCD Panel HPD & AUX strapping

C8350 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8351 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8352 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8353 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8354 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8355 9.1PF ±/-0.1PF C0G-CERM 0201 50V

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

R8300 0 5% 1/20W MF 0201

LCD_HPD
LCD_FSS

DP_INT_AUXCH_C_P C8328 0.1UF 10% 16V X5R-CERM 0201
DP_INT_AUXCH_C_N C8329 0.1UF 10% 16V X5R-CERM 0201

DP_INT_ML_C_P<0> C8320 0.1UF
DP_INT_ML_C_N<0> C8321 0.1UF
DP_INT_ML_C_P<1> C8322 0.1UF
DP_INT_ML_C_N<1> C8323 0.1UF
DP_INT_ML_C_P<2> C8324 0.1UF
DP_INT_ML_C_N<2> C8325 0.1UF
DP_INT_ML_C_P<3> C8326 0.1UF
DP_INT_ML_C_N<3> C8327 0.1UF

DP_INT_ML_F_P<0> DP_INT_ML_F_N<0> DP_INT_ML_F_P<1> DP_INT_ML_F_N<1> DP_INT_ML_F_P<2> DP_INT_ML_F_N<2> DP_INT_ML_F_P<3> DP_INT_ML_F_N<3>

150OHM-100MA-8.5GHZ DLP0NS
CRITICAL FL8300
CRITICAL FL8301
CRITICAL FL8302
CRITICAL FL8303

CRITICAL J8300 20525-130E-01 F-RT-SM

PPVOUT_S0_LCDBKLT
NC
LCD_HPD_CONN
DP_INT_AUX_P
DP_INT_AUX_N
DP_INT_ML_P<0> DP_INT_ML_N<0> DP_INT_ML_P<1> DP_INT_ML_N<1> DP_INT_ML_P<2> DP_INT_ML_N<2> DP_INT_ML_P<3> DP_INT_ML_N<3>

518S0829

EDP_IG_PANEL_PWR

CRITICAL U8300 FPF1009 MFET-2X2-BIN
PP5V_S4
ON
VIN_1 VIN_2 VOUT_1 VOUT_2 GND THERM PAD

C8309 0.1UF 10% 16V X7R-CERM 0402
C8311 0.1UF 10% 16V X7R-CERM 0402
C8312 10UF 20% 6.3V X5R 603

PP5VR3V3_SW_LCD_ISNS
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

SENSOR_NONPROD_R XW8320 SM
NC_ISNS_LCD_PANELN
NC_ISNS_LCD_PANELP

PP5VR3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

CRITICAL L8300 FERR-220-OHM 0805

C8301 0.1UF 10% 16V X7R-CERM 0402
C8302 0.001UF 10% 50V X7R-CERM 0402
C8300 1000PF 10% 100V X7R 0603

PP5VR3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

PP3V3_S0
R8303 1M 5% 1/20W MF 201
R8301 1M 5% 1/20W MF 201
R8302 1M 5% 1/20W MF 201

R8311 1M 5% 1/20W MF 201
R8312 1M 5% 1/20W MF 201
R8313 1M 5% 1/20W MF 201
R8314 1M 5% 1/20W MF 201
R8315 1M 5% 1/20W MF 201
R8316 1M 5% 1/20W MF 201
R8317 1M 5% 1/20W MF 201
R8318 1M 5% 1/20W MF 201

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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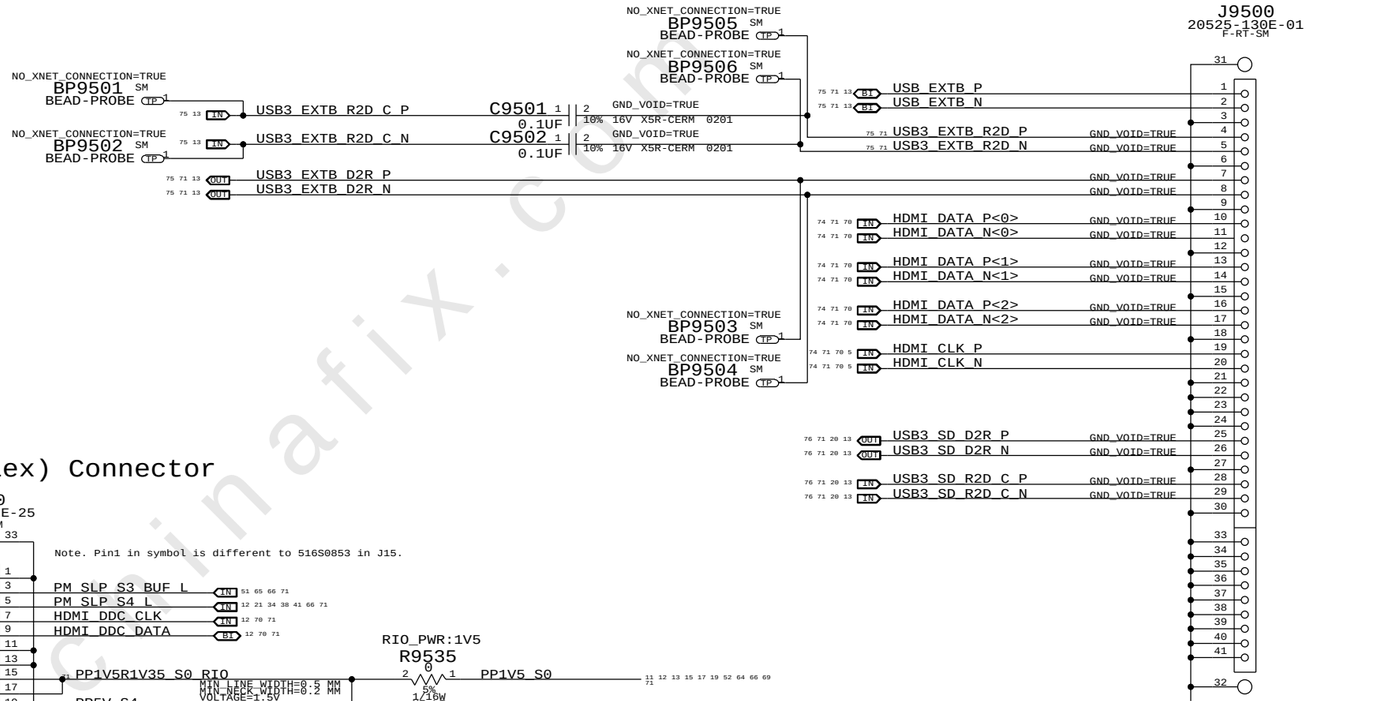
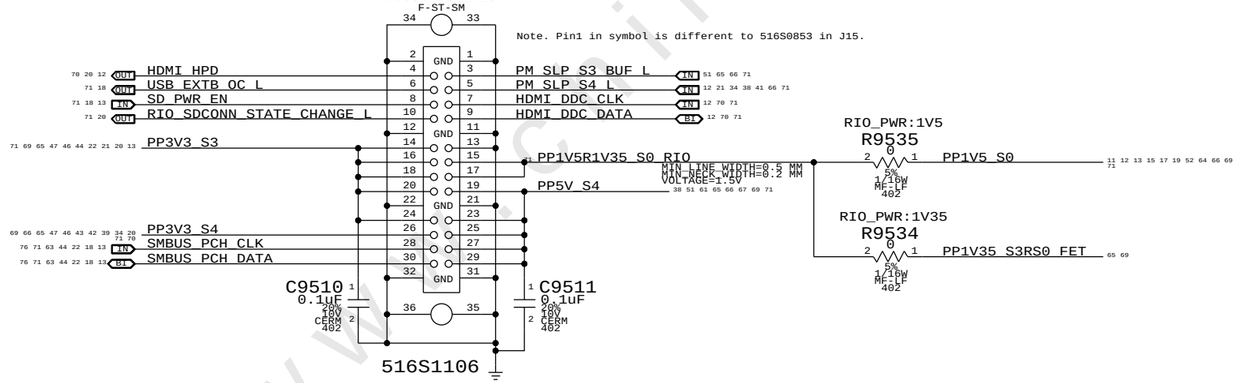
Wire-to-Board (Micro-coax) Connector



Board-to-Board (Flex) Connector



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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: RIO Connectors

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8 7 6 5 4 3 2 1

G3H/5V Rails

PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H

PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS

PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS

PPVIN_S5_HS_OTHER5V_ISNS
PPVIN_S5_HS_OTHER5V_ISNS
PPVIN_S5_HS_OTHER5V_ISNS

PPVIN_S4_TPAD
PPVIN_S4_TPAD
PPVIN_S4_TPAD

PPDCIN_G3H
PPDCIN_G3H
PPDCIN_G3H
PPDCIN_G3H

PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL

PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H

PPVRTC_G3H
PPVRTC_G3H
PPVRTC_G3H

PP5V_S5
PP5V_S5
PP5V_S5

PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4

PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3

PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0

3.3V Rails

PP3V3_S5
PP3V3_S5
PP3V3_S5

Display Aliases

71 70 67 12	EDP_IG_PANEL_PWR	=	EDP_IG_PANEL_PWR	12 67 70 71
71 70 63 12	EDP_IG_BKL_ON	=	EDP_IG_BKL_ON	12 63 70 71
70 63 12	EDP_IG_BKL_PWM	=	EDP_IG_BKL_PWM	12 63 70
74 67 5	DP_INT_ML_C_P<3..0>	=	TP_DP_IG_A_MLP<3..0>	
74 67 5	DP_INT_ML_C_N<3..0>	=	TP_DP_IG_A_MLN<3..0>	
74 70 67 5	DP_INT_AUXCH_C_P	=	DP_INT_AUXCH_C_P	5 67 70 74
74 70 67 5	DP_INT_AUXCH_C_N	=	DP_INT_AUXCH_C_N	5 67 70 74
70 28 12	DP_TBTSNK0_HPD	=	DP_TBTSNK0_HPD	12 28 70
74 28 5	DP_TBTSNK0_ML_C_P<3..0>	=	TP_DP_IG_B_MLP<3..0>	
74 28 5	DP_TBTSNK0_ML_C_N<3..0>	=	TP_DP_IG_B_MLN<3..0>	
74 70 28 12	DP_TBTSNK0_AUXCH_C_P	=	DP_TBTSNK0_AUXCH_C_P	12 28 70 74
74 70 28 12	DP_TBTSNK0_AUXCH_C_N	=	DP_TBTSNK0_AUXCH_C_N	12 28 70 74
70 33 12	DP_TBTSNK0_DDC_DATA	=	DP_TBTSNK0_DDC_DATA	12 33 70
70 33 12	DP_TBTSNK0_DDC_CLK	=	DP_TBTSNK0_DDC_CLK	12 33 70
70 28 12	DP_TBTSNK1_HPD	=	DP_TBTSNK1_HPD	12 28 70
74 28 5	DP_TBTSNK1_ML_C_P<3..0>	=	TP_DP_IG_C_MLP<3..0>	
74 28 5	DP_TBTSNK1_ML_C_N<3..0>	=	TP_DP_IG_C_MLN<3..0>	
74 70 28 12	DP_TBTSNK1_AUXCH_C_P	=	DP_TBTSNK1_AUXCH_C_P	12 28 70 74
74 70 28 12	DP_TBTSNK1_AUXCH_C_N	=	DP_TBTSNK1_AUXCH_C_N	12 28 70 74
70 33 12	DP_TBTSNK1_DDC_DATA	=	DP_TBTSNK1_DDC_DATA	12 33 70
70 33 12	DP_TBTSNK1_DDC_CLK	=	DP_TBTSNK1_DDC_CLK	12 33 70
70 68 20 12	HDMI_HPD	=	HDMI_HPD	12 20 68 70
74 71 68	HDMI_DATA_P<0..2>	=	TP_DP_IG_D_MLP<2..0>	5
74 71 68	HDMI_DATA_N<0..2>	=	TP_DP_IG_D_MLN<2..0>	5
74 71 70 68 5	HDMI_CLK_P	=	HDMI_CLK_P	5 68 70 71 74
74 71 70 68 5	HDMI_CLK_N	=	HDMI_CLK_N	5 68 70 71 74
71 70 68 12	HDMI_DDC_CLK	=	HDMI_DDC_CLK	12 68 70 71
71 70 68 12	HDMI_DDC_DATA	=	HDMI_DDC_DATA	12 68 70 71

MAKE_BASE=TRUE

CPU signals

70 60 21	MEMVTT_EN	=	MEMVTT_EN	21 60 70

MAKE_BASE=TRUE

Thunderbolt Signals Through PEG

74 28 5	PCIE_TBT_D2R_P<3..0> (IN)	=	=PEG_D2R_P<3..0> (OUT)	
74 28 5	PCIE_TBT_D2R_N<3..0> (IN)	=	=PEG_D2R_N<3..0> (OUT)	
74 28 5	PCIE_TBT_R2D_C_P<3..0> (OUT)	=	=PEG_R2D_C_P<3..0> (IN)	
74 28 5	PCIE_TBT_R2D_C_N<3..0> (OUT)	=	=PEG_R2D_C_N<3..0> (IN)	

MAKE_BASE=TRUE

Unused PEG Lanes

5	TP_PEG_D2RP<15..4>	=	=PEG_D2R_P<15..4>
5	TP_PEG_D2RN<15..4>	=	=PEG_D2R_N<15..4>
5	TP_PEG_R2D_CP<15..4>	=	=PEG_R2D_C_P<15..4>
5	TP_PEG_R2D_CN<15..4>	=	=PEG_R2D_C_N<15..4>

MAKE_BASE=TRUE

70 49	PP3V3_S3_FAN_CTL	=	PP3V3_S3_FAN_CTL	49 70	MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=3.3V MAKE_BASE=TRUE

RA201: 0, 1/20W MF 0201, 5%, 1 — 2: PP3V3_S5 (12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 71 81)

RA202: 0, 1/20W MF 0201, 5%, 1 — 2: PP3V3_S4 (20 34 39 42 43 46 47 65 66 68 69 71); NOSTUFF

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
14	DPMUX_UC_IRQ
11	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L

		VOLTAGE	MAKE_BASE			
77 74 70 24 23 22	PP0V75_S3_MEM_VREFDQ_A	= 0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 74 77	
74 70 26 25 22	PP0V75_S3_MEM_VREFDQ_B	= 0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70 74	
77 74 70 24 23 22	PP0V75_S3_MEM_VREFCA_A	= 0.675V	TRUE	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 74 77	
74 70 26 25 22	PP0V75_S3_MEM_VREFCA_B	= 0.675V	TRUE	PP0V75_S3_MEM_VREFCA_B	22 25 26 70 74	

65 63 62 59 58 50 49 37 19 18 71 69 66 PP5V_S0

XWA202 SM 1 — 2: PP5V_S0_AUDIO_AMP_L (53) MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V

XWA203 SM 1 — 2: PP5V_S0_AUDIO_AMP_R (53) MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Signal Aliases

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Functional Test Points

J3501 - airport

FUNC_TEST		
TRUE	AP_CLKREQ_Q_L	34
TRUE	AP_RESET_CONN_L	34
TRUE	PCIE_AP_D2R_PI_N	34 76
TRUE	PCIE_AP_D2R_PI_P	34 76
TRUE	PCIE_AP_R2D_N	34 76
TRUE	PCIE_AP_R2D_P	34 76
TRUE	PCIE_CLK100M_AP_CONN_N	34 76
TRUE	PCIE_CLK100M_AP_CONN_P	34 76
TRUE	PCIE_WAKE_L	12 34 36 76
TRUE	PP3V3_S3RS4_BT_F	34
TRUE	PP3V3_WLAN	34 42
TRUE	USB_BT_CONN_N	34 75
TRUE	USB_BT_CONN_P	34 75
TRUE	WIFI_EVENT_L	34 41 42
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	37 79
TRUE	MIPI_CLK_CONN_P	37 79
TRUE	CAM_SENSOR_WAKE_L_CONN	37
TRUE	MIPI_DATA_CONN_N	37 79
TRUE	MIPI_DATA_CONN_P	37 79
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 80
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 80
TRUE	I2C_CAM_SCK	36 37
TRUE	I2C_CAM_SDA	36 37
TRUE	PP5V_S3RS0_ALSCAM_F	37
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	5 68 70 74
TRUE	HDMI_CLK_P	5 68 70 74
TRUE	HDMI_DATA_N<0>	68 70 74
TRUE	HDMI_DATA_N<1>	68 70 74
TRUE	HDMI_DATA_N<2>	68 70 74
TRUE	HDMI_DATA_P<0>	68 70 74
TRUE	HDMI_DATA_P<1>	68 70 74
TRUE	HDMI_DATA_P<2>	68 70 74
TRUE	USB3_SD_D2R_N	13 20 68 76
TRUE	USB3_SD_D2R_P	13 20 68 76
TRUE	USB3_SD_R2D_C_N	13 20 68 76
TRUE	USB3_SD_R2D_C_P	13 20 68 76
TRUE	USB3_EXTB_D2R_N	13 68 75
TRUE	USB3_EXTB_D2R_P	13 68 75
TRUE	USB3_EXTB_R2D_N	68 75
TRUE	USB3_EXTB_R2D_P	68 75
TRUE	USB_EXTB_N	13 68 75
TRUE	USB_EXTB_P	13 68 75
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 68
TRUE	PP1V5R1V35_S0_RIO	68
TRUE	HDMI_DDC_CLK	12 68 70
TRUE	HDMI_DDC_DATA	12 68 70
TRUE	HDMI_HPD_L	
TRUE	SMBUS_PCH_CLK	13 18 22 44 63 68 76
TRUE	SMBUS_PCH_DATA	13 18 22 44 63 68 76
TRUE	PM_SLP_S3_BUF_L	51 65 66 68
TRUE	PM_SLP_S4_L	12 21 34 38 41 66 68
TRUE	PP3V3_S3	3X 13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S4	5X 38 51 61 65 66 67 68 69
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 68
TRUE	USB_EXTB_OC_L	18 68
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	SMC_LID_R	43
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6100 - lpc + spi

FUNC_TEST		
TRUE	LPCPLUS_GPIO	14 50
TRUE	LPCPLUS_RESET_L	20 50 76
TRUE	LPC_AD<0>	13 41 50 76
TRUE	LPC_AD<1>	13 41 50 76
TRUE	LPC_AD<2>	13 41 50 76
TRUE	LPC_AD<3>	13 41 50 76
TRUE	LPC_CLK33M_LPCPLUS	19 50 76
TRUE	LPC_FRAME_L	13 41 50 76
TRUE	LPC_PWRDWN_L	12 20 41 50
TRUE	LPC_SERIRQ	13 41 50
TRUE	PM_CLKRUN_L	12 41 50
TRUE	PP5V_S0	18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	SMC_RESET_L	41 42 50 57
TRUE	SMC_ROMBOOT	42 50
TRUE	SMC_RX_L	41 42 50
TRUE	SMC_TCK	41 42 50
TRUE	SMC_TDI	41 42 50
TRUE	SMC_TDO	41 42 50
TRUE	SMC_TMS	41 42 50
TRUE	SMC_TX_L	41 42 50
TRUE	SPIROM_USE_MLB	14 50
TRUE	SPI_ALT_CLK	50
TRUE	SPI_ALT_CS_L	50
TRUE	SPI_ALT_MISO	50
TRUE	SPI_ALT_MOSI	50
TRUE	TP_SMC_MD1	50
TRUE	TP_SMC_TRST_L	50
TRUE	GND	2X

J4800 - ipd flex

TRUE	Z2_CS_L	39
TRUE	Z2_MOSI	39
TRUE	Z2_MISO	39
TRUE	Z2_SCLK	39
TRUE	Z2_HOST_INTN	39
TRUE	Z2_CLKIN	39
TRUE	Z2_KEY_ACT_L	39
TRUE	PSOC_F_CS_L	39
TRUE	PICKB_L	39
TRUE	PSOC_MOSI	39
TRUE	PSOC_MISO	39
TRUE	PSOC_SCLK	39
TRUE	SMBUS_SMC_2_S3_SCL	39 41 44 80
TRUE	SMBUS_SMC_2_S3_SDA	39 41 44 80
TRUE	SMC_LID	39 41 42 43
TRUE	SMC_T101_COM_1	
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S5	39 61 65 69 71
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	WS_CONTROL_KBD	39
TRUE	WS_KBD1	39
TRUE	WS_KBD10	39
TRUE	WS_KBD11	39
TRUE	WS_KBD12	39
TRUE	WS_KBD13	39
TRUE	WS_KBD14	39
TRUE	WS_KBD15_CAP	39
TRUE	WS_KBD16_NUM	39
TRUE	WS_KBD17	39
TRUE	WS_KBD18	39
TRUE	WS_KBD19	39
TRUE	WS_KBD2	39
TRUE	WS_KBD20	39
TRUE	WS_KBD21	39
TRUE	WS_KBD22	39
TRUE	WS_KBD23	39
TRUE	WS_KBD3	39
TRUE	WS_KBD4	39
TRUE	WS_KBD5	39
TRUE	WS_KBD6	39
TRUE	WS_KBD7	39
TRUE	WS_KBD8	39
TRUE	WS_KBD9	39
TRUE	WS_KBD_ONOFF_L	39
TRUE	WS_LEFT_OPTION_KBD	39
TRUE	WS_LEFT_SHIFT_KBD	39
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 40 63
TRUE	KBDBKLT_RETURN2	2X 40 63
TRUE	PPVOUT_S0_KBDBKLT	40 63
TRUE	GND	4X

J6701 - audio flex

FUNC_TEST		
TRUE	AUD_HP_PORT_L	51 55
TRUE	AUD_HP_PORT_R	51 55
TRUE	AUD_SPDIF_OUT_JACK	
TRUE	AUD_TIPDET_INV	
TRUE	AUD_TYPEDET	51 55
TRUE	AUD_CONN_MIC_XW	4X
TRUE	CH_HS_MIC	
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	AUD_CONN_SLEEVE_XW	4X 54 55
TRUE	US_HS_MIC	
TRUE	GND	2X GND

J6601 - mic

TRUE	DMIC_CLK3	52 55
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	DMIC_SDA2	55
TRUE	DMIC_SDA3	52 55
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	52 55
TRUE	SPKRCONN_L_OUT_N	53 55 81
TRUE	SPKRCONN_L_OUT_P	53 55 81
TRUE	SPKRCONN_SL_OUT_N	53 55 81
TRUE	SPKRCONN_SL_OUT_P	53 55 81
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	52 55
TRUE	SPKRCONN_R_OUT_N	53 55 81
TRUE	SPKRCONN_R_OUT_P	53 55 81
TRUE	SPKRCONN_SR_OUT_N	53 55 81
TRUE	SPKRCONN_SR_OUT_P	53 55 81
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	41 44 56 57 80
TRUE	SMBUS_SMC_5_G3_SDA	41 44 56 57 80
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	67 74
TRUE	DP_INT_AUX_P	67 74
TRUE	DP_INT_ML_N<0>	67 74
TRUE	DP_INT_ML_N<1>	67 74
TRUE	DP_INT_ML_N<2>	67 74
TRUE	DP_INT_ML_N<3>	67 74
TRUE	DP_INT_ML_P<0>	67 74
TRUE	DP_INT_ML_P<1>	67 74
TRUE	DP_INT_ML_P<2>	67 74
TRUE	DP_INT_ML_P<3>	67 74
TRUE	LCD_FSS	63 67
TRUE	LCD_HPD_CONN	67
TRUE	LED_RETURN_1	63 67
TRUE	LED_RETURN_2	63 67
TRUE	LED_RETURN_3	63 67
TRUE	LED_RETURN_4	63 67
TRUE	LED_RETURN_5	63 67
TRUE	LED_RETURN_6	63 67
TRUE	PP5VR3V3_SW_LCD	3X 67
TRUE	PPVOUT_S0_LCDBKLT	63 67
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 41 66
TRUE	PPVTT_S0_DDR	21 27 60 69
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	PP3V3_S3	13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 81
TRUE	PP3V3_S5_AVREF_SMC	41 42
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	PP5V_S0	18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	PP5V_S3	21 37 60 65 66 69
TRUE	PP5V_S5	39 61 65 69 71
TRUE	PPBUS_G3H	30 45 56 57 63 69
TRUE	PPDCIN_G3H	56 57 69
TRUE	PPVCC_S0_CPU	6 8 10 46 59 69
TRUE	PPVTTDDR_S3	60 69
TRUE	PP3V3_S0SW_SSD	35 46 69
TRUE	PP1V5_S0	11 12 13 15 17 19 52 64 66 68 69
TRUE	PP1V35_S3	21 22 46 60 65 69

XDP

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 18 74
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 74
TRUE	XDP_CPU_TDO	6 18 74
TRUE	XDP_CPUPCH_TRST_L	6 18 74
TRUE	XDP_CPU_TMS	6 18 74
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 74
TRUE	XDP_CPU_PRDY_L	6 18 74
TRUE	PM_RSMRST_L	12 66 76
TRUE	PM_PCH_PWROK	12 19 76
TRUE	PM_SYSRST_L	12 19 41 76
TRUE	CPU_CFG<3>	6 18 74
TRUE	PP1V05_S0	14 15 17 18 42 62 66 69
TRUE	GND	2X GND

Power Sequence

FUNC_TEST		
TRUE	SMC_ONOFF_L	39 41 42
TRUE	PM_DSW_PWRGD	12 41 76
TRUE	ALL_SYS_PWRGD	18 19 41 58 66
TRUE	PM_PCH_SYS_PWROK	12 18 19 41 76
TRUE	PLT_RESET_L	12 18 20 21
TRUE	EDP_IG_PANEL_PWR	12 67 70
TRUE	EDP_IG_BKL_ON	12 63 70

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NC NO_TESTs

PCH

	NO_TEST	MAKE_BASE	
NC_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN	TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP	TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN	TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP	TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP	TRUE	TRUE	NC_USB3_EXTD_R2D_CP
NC_PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
NC_SATA_A_D2RN	TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP	TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN	TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP	TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN	TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP	TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN	TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP	TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP
NC_USB_EXTCN	TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP	TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN	TRUE	TRUE	NC_USB_SDN
NC_USB_SDP	TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
NC_USB_6N	TRUE	TRUE	NC_USB_6N
NC_USB_6P	TRUE	TRUE	NC_USB_6P
NC_USB_7N	TRUE	TRUE	NC_USB_7N
NC_USB_7P	TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN	TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP	TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN	TRUE	TRUE	NC_USB_IRN
NC_USB_IRP	TRUE	TRUE	NC_USB_IRP
NC_ITPXDP_CLK100MN	TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP	TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L
NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN
NC_SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

	NO_TEST	MAKE_BASE	
NC_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT
TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
NC_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP
NC_PCIE_CLK100M_GPUN	TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP	TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
NC_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
NC_USB_4N	TRUE	TRUE	NC_USB_4N
NC_USB_4P	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>	28 74
TRUE	PCIE_TBT_R2D_N<3..0>	28 74
TRUE	PCIE_TBT_D2R_C_P<3..0>	28 74
TRUE	PCIE_TBT_D2R_C_N<3..0>	28 74
TRUE	DMI_S2N_P<3..1>	5 12 74
TRUE	DMI_S2N_N<3..1>	5 12 74
TRUE	DMI_N2S_P<3..1>	5 12 74
TRUE	DMI_N2S_N<3..1>	5 12 74

PLACEABLE BEAD-PROBES FOR TBT

TBT_A_R2D_C_P<1>	1	SM	BEAD-PROBE BPA535 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_P<1>	1	SM	BEAD-PROBE BPA531 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	1	SM	BEAD-PROBE BPA532 NO_XNET_CONNECTION=TRUE

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J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_P<3:0>	5 12 72
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_N<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_P<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_N<3:0>	5 12 72
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 71
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 72
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 72
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 71
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 71
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 71
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 71
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 71
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 71
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 71
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 41
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 41 42 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTI	PM_THRMTRIP_L	6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	22 25 26 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 70
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 72
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 72
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 70
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 70

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 67 70
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 67 70
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 71
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 71

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	68 70 71
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	5 68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	5 68 70 71
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 28 70
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 28 70
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 28 70
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 28 70
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
	DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 70
	DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 70
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
	DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 70
	DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 70

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 72
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 72
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 72
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 72
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 72
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 72
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 72
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 72
T213 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_85D	USB	USB_EXTA_P	13 38
	USB_85D	USB	USB_EXTA_N	13 38
T24	USB_85D	USB	USB_EXTA_MUXED_P	38
T24	USB_85D	USB	USB_EXTA_MUXED_N	38
T23	USB_85D	USB	USB_LT1_P	38
T23	USB_85D	USB	USB_LT1_N	38
	USB_85D	USB	NC_USB_EXTCP	13 72
	USB_85D	USB	NC_USB_EXTCN	13 72
T23	USB_85D	USB	NC_USB_SDP	13 72
T23	USB_85D	USB	NC_USB_SDN	13 72
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
USB_SMC	USB_85D	USB	NC_USB_SMCP	72
USB_SMC	USB_85D	USB	NC_USB_SMCN	72
T28	USB_85D	USB	NC_USB_6P	13 72
T28	USB_85D	USB	NC_USB_6N	13 72
T28	USB_85D	USB	NC_USB_7P	13 72
T28	USB_85D	USB	NC_USB_7N	13 72
	USB_85D	USB	USB_EXTB_P	13 68 71
	USB_85D	USB	USB_EXTB_N	13 68 71
T26	USB_85D	USB	NC_USB_EXTDP	13 72
T25	USB_85D	USB	NC_USB_EXTDN	13 72
	USB_85D	USB	USB_BT_P	13 34
	USB_85D	USB	USB_BT_N	13 34
	USB_85D	USB	USB_BT_CONN_P	34 71
	USB_85D	USB	USB_BT_CONN_N	34 71
T28	USB_85D	USB	NC_USB_IRP	13 72
T28	USB_85D	USB	NC_USB_IRN	13 72
T28	USB_85D	USB	USB_TPAD_P	13 39
T28	USB_85D	USB	USB_TPAD_N	13 39
T30	USB_85D	USB	USB_TPAD_R_P	39
T30	USB_85D	USB	USB_TPAD_R_N	39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
T22 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
T23 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
T23 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
T22 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 68 71
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 68 71
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	68 71
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	68 71
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 68
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 68
T28 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 72
T28 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 72
T28	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 72
T28	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 72
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 72
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 72
T29	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 72
T29	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 72

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T256 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
T255 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
T255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
T255 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
T253 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
T256	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41 50 71
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41 50 71
LPC_RESET_L	LPC_45S	LPC	LPCPLUS_RESET_L	20 50 71
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 22 44 63 68 71
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 22 44 63 68 71
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
	HDA_45S	HDA	HDA_BIT_CLK_R	11
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
	HDA_45S	HDA	HDA_SYNC_R	11
	HDA_45S	HDA	HDA_RST_R_L	11
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
	HDA_45S	HDA	HDA_SDOUT_R	11 19
	SPI_45S	SPI	SPI_CLK_R	13 50
SPI_CLK	SPI_45S	SPI	SPI_CLK	50
	SPI_45S	SPI	SPI_MOSI_R	13 50
SPI_MOSI	SPI_45S	SPI	SPI_MOSI	50
SPI_MISO	SPI_45S	SPI	SPI_MISO	13 50
	SPI_45S	SPI	SPI_CS0_R_L	13 50
SPI_CS0	SPI_45S	SPI	SPI_CS0_L	50
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 68 71
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 68 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 71
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
[180]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
[180]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
[179]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 71
[179]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 71
[175] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
[175] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
[174]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
[174]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
[175] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
[175] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
[33]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
[33]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 50 71
[50]	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
[43] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
[254] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
[255] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
[253] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
[254] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
[257] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
[258] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
[255] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
[257] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
[256] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
[256] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
[180]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 71
[179]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 71
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
[33]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
[33]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
[285] PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
[285]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
[315] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
[315] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
[315] PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
[315] PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
[308] PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 66 71
[307] PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 71
[315] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
[314] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
[320] PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 71
[315] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 71
[307] PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
[306] PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
[326] PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 71
[172] PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
[335] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>	13 35
[336] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>	13 35
[338] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>	13 35
[337] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>	13 35
[338]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>	35
[334]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>	35

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A 22 23 24 78 74
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A 22 23 24 78 74
		MEM_PWR	PP1V35_S3_MEM 23 24 25 26 46 69

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING
TBT_A_R2D	TBTDP_85D	TBTDP_R2D
DP_A_LSX_ML	DP_85D	DISPLAYPORT
DP_TBTPA_ML	DP_85D	DISPLAYPORT
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R
TBT_A_AUXCH	DP_85D	

TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0>	28 31 72
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0>	28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0>	31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0>	28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0>	28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1>	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1>	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1>	28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1>	28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N	31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P	28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N	28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P	31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N	31

TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0>	28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0>	28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0>	32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0>	28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1>	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1>	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N	32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P	28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N	28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P	32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N	32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING
	DP_85D	DISPLAYPORT
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI

	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	28

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 36 37
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 36 37
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 36 37
1101	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 36 37
1102		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 37
1103	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 36 37
1104	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 36 37
1105	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 36 37
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 36 37
1106	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 36 37
1107	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 36 37
1108	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 36 37
1109	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 36 37
1110	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 36 37
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 36 37
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 36 37
1127	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 36 37
1128	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 36 37
1129		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 37 71
1130		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 37 71
1131	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 36 37
1132	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 36 37
1133		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 37 71
1134		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 37 71
1135			S2_MEM_PWR	PP1V35_CAM 36 37
1136			S2_MEM_PWR	PP0V675_CAM_VREF 36 37
1138			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 37
1139			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 37

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 71
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 71
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 71
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 71
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	41 44 56 57 71
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 71
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	47
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	46
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N	46 59
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_N	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	62
	THERM_1TO1_45S	THERM	P1V05S0_CS_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P	62
	THERM_1TO1_45S	THERM	P1V05S0_SENSE_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	28 48
	THERM_1TO1_45S	THERM	TBT_THERMD_N	48
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N	47

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
	AUDIODIFF	AUDIO	RSUBIN_P	53
	AUDIODIFF	AUDIO	RSUBIN_N	53
	AUDIODIFF	AUDIO	LSUBIN_P	53
	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 71
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 71
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 71
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 71
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 71
	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
	DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
	DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
	DIFFPAIR	AUDIO	HS_MIC_P	51 54
	DIFFPAIR	AUDIO	HS_MIC_N	51 54
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53
		SB_POWER	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 71
		SB_POWER	PP3V3_S0	60 66 67 11 12 13 14 15 17 19 20 25 33 36 44 45 46 47 48 49 51 52 55 60 71 8 10 21 65 66 69
		SB_POWER	PP1V35_S3RS0_CPUDDR	
		GND	GND	

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